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High-Performance Single-Active-Layer Memristor Based on an Ultrananocrystalline Oxygen-Deficient TiO_x Film

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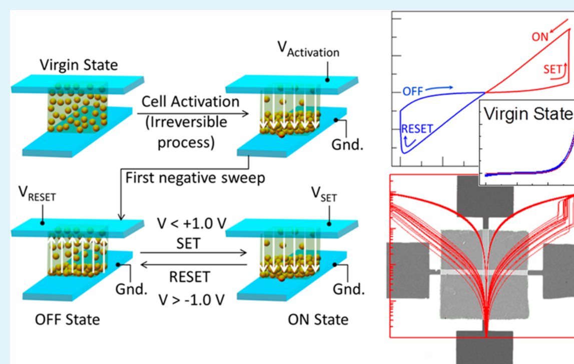
Supporting Information

ABSTRACT: The theoretical and practical realization of memristive devices has been hailed as the next step for nonvolatile memories, low-power remote sensing, and adaptive intelligent prototypes for neuromorphic and biological systems. However, the active materials of currently available memristors need to undergo an often destructive high-bias electroforming process in order to activate resistive switching. This limits their device performance in switching speed, endurance/retention, and power consumption upon high-density integration, due to excessive Joule heating. By employing a nanocrystalline oxygen-deficient TiO_x switching matrix to localize the electric field at discrete locations, it is possible to resolve the Joule heating problem by reducing the need for electroforming at high bias. With a $Pt/TiO_x/Pt$ stacking architecture, our device follows an electric field driven, vacancy-modulated interface-type switching that is sensitive to the junction size. By scaling down the junction size, the SET voltage and output current can be reduced, and a SET voltage as low as +0.59 V can be obtained for a 5×5 μm^2 junction size. Along with its potentially fast switching (over 10^5 cycles with a 100 μs voltage pulse) and high retention (over 10^5 s) performance, memristors based on these disordered oxygen-deficient TiO_x films promise viable building blocks for next-generation nonvolatile memories and other logic circuit systems.



KEYWORDS: *nonvolatile memories, single-active-layer memristors, oxygen-vacancy defect rich ultrananocrystallites, interface-type switching, electroforming-free*

INTRODUCTION

Resistive random access memory (ReRAM) or memristor, based on transition metal oxides, has been demonstrated as the fourth passive circuit element with potential application as the next-generation nonvolatile memory device.[1−11] Properties such as low power consumption,[12,13] subnanosecond switching speed,[14−17] and high switching endurance[4,5,18,19] make the memristor an attractive candidate as the main building block for such adaptive systems as logic circuits, neuromorphic devices, and artificial biological systems. With a simple metal/semiconductor−oxide/metal architecture, the memristor operates on the principle of binary resistive switching[20,21] between two discrete resistance states, mediated by an ionic transport process. Inspired by the first successful fabrication of a TiO_2 based memristor by Strukov et al. in 2008,[3] a large class of transition metal oxides[4,5,13,22−31] along with chalcogenides[32] and organic polymers[33] have since been demonstrated as viable switching materials. As this has become an active research area in the past few years, there emerge two popular switching mechanisms, involving formation/dissolution of one or more conducting filaments (filament-type switching)[5,6,26] vs electromigration of oxygen vacancies driven by an applied electric field (interface-type switching).[4,25] Filament-type switching is a widely accepted mechanism for transition-metal oxide based memristors.[7,34−37] The idea is based on the emergence of one or more vertical columns (filaments) of a more conducting oxide phase[5,38,39] or even a metallic phase,[40] with widths of a few nanometers, through the semiconducting oxide layer.[25,41] The formation and dissolution of these filaments are dominated by Joule heating,[21,22,42,43] as the voltage to the device is cycled through the high and low resistance states. Such a process requires an irreversible electroforming process induced by a high bias (generally greater than ±10 V) to break bonds in the metal oxide in order to create a temperature-dependent, oxygen-vacancy-defect-rich conducting phase.

Resistive switching can also be achieved by ionic drift of the electronically charged oxygen vacancies between the two metal−insulator (oxide) interfaces driven by an electric field gradient, thereby controlling the resistance states of the device.[4] In this case, the switching occurs between two different oxygen vacancy concentrations created by an activation process, but the excess oxygen can diffuse into the electrode causing corrosion and even device blow-up during gas release out of the junction.[5] This process is described as interface-type switching, where the oxygen vacancies migrate toward or away from the interface (depending on the voltage polarity) through an oxygen-

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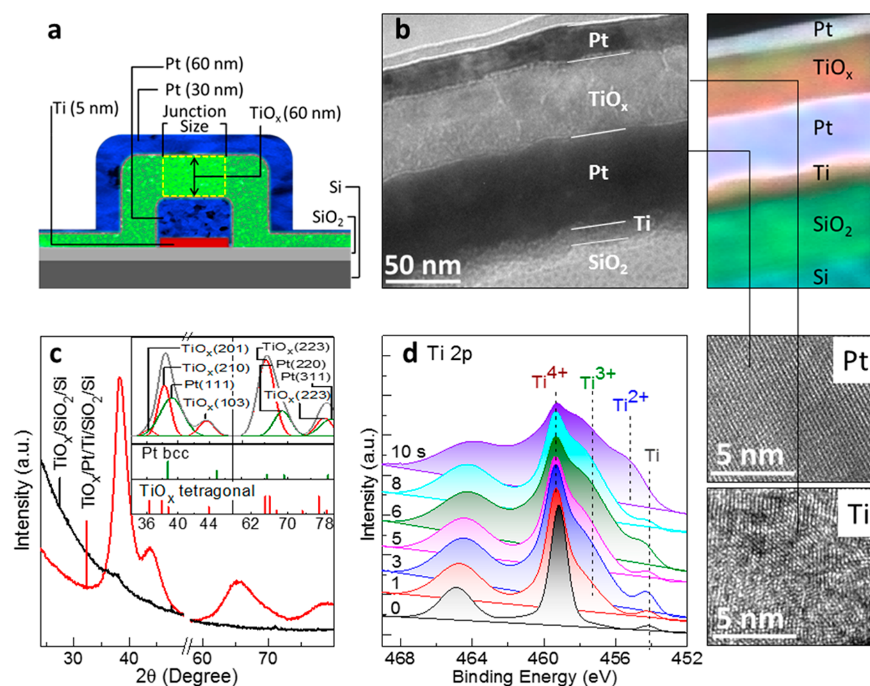

Figure 1. Physical characterization for TiO_x based memristive devices. (a) Schematic cross-sectional view of the $Pt/TiO_x/Pt$ device architecture supported on a SiO_2/Si substrate. (b) TEM image of a cross-section of a typical memristive device, with the corresponding EDX elemental maps (top right) and high-resolution TEM images of selected Pt and TiO_x regions (bottom right). For each device, the layer thickness of the top Pt electrode is 30 nm, while those for the TiO_x active layer and the bottom Pt electrode are 60 nm. A 5 nm thick Ti layer is also predeposited immediately before depositing the bottom Pt layer electrode on the SiO_2/Si substrate in order to provide better Pt adhesion to the substrate. (c) XRD profile and (d) depth-profiling XPS spectra of the Ti 2p region of a TiO_x film as-deposited on the Pt bottom electrode predeposited with a Ti adhesion layer, all supported on a SiO_2/Si substrate, shown along with the reference patterns for Pt FCC (PDF# 01-087-0644) and TiO_x tetragonal phase (PDF# 00-008-0386) in c and with the binding energy locations of relevant Ti ionic states in d. As Ti^{n+} (in TiO_x) could be reduced to metallic Ti by ion sputtering, we limit the sputtering to no more than 10 s. Precise manipulation of the Ar gas flow rate provides good control of the oxygen vacancy defect concentration to make the TiO_x active layer appropriate for electronic transport. The XRD profile is expanded in two different 2θ regions (34−46° and 58−80°) in the inset of c. The XRD profile of a TiO_x film deposited on the SiO_2/Si substrate is also shown in c for comparison.

vacancy-defect-rich conducting conduit covering the size of the entire device junction. While a very high electric field (10^6 V cm^{-1})[44] is generally required to move these vacancies in bulk material, such a field can be created by applying just a few volts (6−10 V) across a few nanometer thick film in a device. Depending on the nature of the switching and electrode materials and the layer stacking arrangement, the switching mechanism could be thermal dominating (filament type) or electric-field dominating (interface type). Of the various obstacles to fabricating a practical memristive device, the high-bias electroforming step is recognized as the root cause behind the poor reproducibility and short lifetime of the memristor.[7,25,45] This high-bias electroforming step is accompanied by correspondingly high Joule heating, leading to poor resistive switching endurance, low reproducibility, and even potential destruction of the device.[5,46] While Joule heating cannot be avoided completely during resistive switching, it should be reduced as much as possible in order to ensure the reliability of the memristors. Furthermore, the formation and dissolution of the filamentary channel(s) could vary from sample to sample in an unpredictable fashion, which leads to unreliable performance. These remain to be the major challenges, and there is therefore an urgent need for a new strategy that could mitigate the adverse Joule heating effect and enable the device to electroform/activate at a much lower applied bias while reducing the power consumption.

Here, we report a novel interface-type-switching memristive device comprising an oxygen-vacancy-defect-rich TiO_x ($1 \leq x < 2$) ultrananocrystalline film with nanocrystallite size of 3−4 nm, stacked between a top and a bottom Pt electrodes. Unlike earlier studies, most of which have focused on starting with a "perfect" (dense, near single-crystalline and phase-pure) TiO_2 material followed by introducing defects such as oxygen vacancies via postannealing, our approach is to introduce defects (such as grain boundaries and oxygen vacancies) directly during film growth. Earlier work[47] has shown that some oxygen vacancies in TiO_2 can be "pinned" in a defect-rich matrix, leading to less mobility and better temperature stability than those introduced by simply annealing in an oxygen-poor atmosphere. By growing a defect-rich nanocrystalline TiO_x film at room temperature, these intrinsic oxygen vacancies have become less mobile, producing highly active nonstoichiometric regions within the film. We hypothesize that this type of defect-rich TiO_x film could have several advantages in a conventional, single-active-layer memristive device. First, the defect-rich matrix could act as a reservoir for excess oxygen, as the device cycles between the high and low resistance states. Second, within the interface-type switching model of conduction, nanoscale variations in TiO_x could promote variations in the local electric fields, enabling the creation of a low resistance region with just a small activation voltage. We demonstrate, for the first time, dynamic resistive switching of a high-performance TiO_x-based memristor, in which an applied bias as low as +1.5 V (one of the lowest activation voltages reported in recent literature, Supporting Information Table S1) is sufficient to create an electric field gradient large enough to switch the

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resistance state of the device from its virgin state. With the nonlinear (Schottky) OFF state and linear (Ohmic) ON state, this device also shows stable nonvolatile bipolar switching characteristics with a high ON-to-OFF current ratio and low power consumption, within a programmable READ voltage range of ±1.0 V and less. This device provides not only greater control and reliability but also higher reproducibility in its endurance and retention capacities. This type of defect-rich TiO_x film demonstrates the value and importance of defects in developing the high performance expected for the next generation of ReRAM devices. These two-terminal single-active-layer devices and their crossbar architecture also offer simplicity in fabrication, while their highly tunable size range (particularly of the switching matrix) ensures scalability and high density device integration.

■ RESULTS AND DISCUSSION

Device Fabrication and Characterization. The crossbar device architecture is fabricated on a SiO_2/Si substrate with four typical junction sizes (5 × 5 μm^2, 10 × 10 μm^2, 20 × 20 μm^2, and 50 × 50 μm^2, Figure 1a and Figure S-1). Cross-sectional TEM and EDX analysis (Figure 1b) validate the as-grown architecture. The high-resolution TEM images further show an ordered crystalline Pt layer and a disordered defect-rich nanocrystalline TiO_x layer, with grain sizes of 2−3 nm in diameter. Glancing incidence XRD data of the TiO_x/Pt/Ti film as-grown on Si (Figure 1c, inset) reveal peaks characteristic of metallic Pt and a stable oxygen-deficient TiO_x phase (PDF# 00-008-0386), discernibly different from the more commonly observed rutile or anatase phase. The corresponding broad peak widths are consistent with the highly defective nature and nanocrystalline size of the TiO_x grains. Scherrer analysis of the peak widths of the TiO_x phase shows a crystallite size of 4−5 nm, in good accord with the TEM data. The XRD profile for TiO_x on SiO_2/Si shows largely amorphous nature with a very weak tetragonal TiO_x (210) peak. XPS (Figure 1d and Figure S-2) and SIMS studies (Figure S-3) further indicate the oxygen-vacancy-defect-rich nature of the films. In the Ti 2p spectra for the TiO_x/Pt structure (i.e., before depositing the top Pt electrode, Figure 1d), the substantially larger moiety of the Ti^{4+} feature before sputtering is consistent with the complete oxidation of the surface region of the TiO_x film under ambient conditions. For the corresponding spectra for the Pt/TiO_x/Pt structure shown in Figure S-2a, other Ti^{n+} features are evidently quite sizable relative to Ti^{4+} in the near surface (upon a short sputtering that removes the top Pt electrode shown in Figure S-2b). The broad Ti $2p_{3/2}$ band between the intense Ti^{4+} feature at 459.3 eV and the weak metallic feature at 454.3 eV that emerges after very brief sputtering (Figure 1d) could be attributed to the presence of Ti^{3+} (at 457.6 eV) and Ti^{2+} (at 455.3 eV). While Ti^{n+} (in a TiO_2 powder standard) is known to get reduced to metallic Ti upon ion sputtering for a few minutes,[46] our TiO_x films exhibit strong Ti^{3+} and Ti^{2+} features after sputtering for just 10 s. The increasing strengths of these latter features with brief sputtering therefore show the presence of highly oxygen-deficient TiO_x in the near surface. The high density of oxygen vacancies in the as-deposited film is further confirmed by the increased transmittance from 8% to 30% in the 400−600 nm region of the UV−vis spectrum upon annealing (Figure S-4).

Resistive Switching and Switching Mechanism. Prior to any applied bias, the TiO_x film stays in the virgin state, exhibiting very high resistance in the MΩ range, with oxygen vacancies distributed uniformly throughout the film thickness. The conduction mechanism of the device in the virgin state is therefore governed by the low oxygen vacancy concentration at the Pt/TiO_x interface. It leads to Schottky-like rectifying behavior in the current−voltage ($I-V$) curve, with exponential dependence corresponding to the thermionic emission model[8,49] (Figure S-5a), over the ±1.0 V range (Figure 2a,

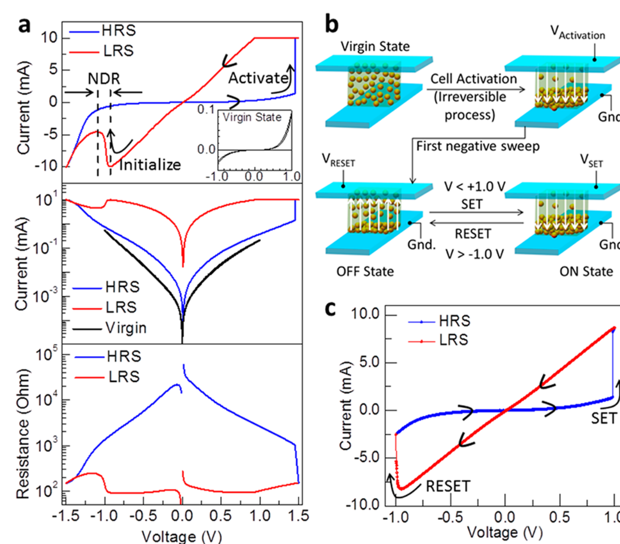

Figure 2. Memristive switching characteristics and mechanism of a typical Pt/TiO_x/Pt device. (a) (Upper) Current (I) vs voltage (V) curve for the first positive (activation) sweep involving resistive switching at an activation voltage of +1.5 V. To ensure safe operation of the device, a compliance current is set to 10 mA. In the first negative (initialization) sweep, the voltage-controlled negative differential resistance (NDR) observed between −0.92 and −1.08 V is due to the inhomogeneity in the electric field caused by the vacancy gradient. The inset shows the same $I-V$ curve for the virgin state of the device (prior to device activation). (Middle) $|I|$ vs V profiles (with $|I|$ in a semilog scale) for the virgin and activation states and (lower) corresponding resistance vs V profile for the high resistance state (HRS) and low resistance state (LRS) in the activation step. The resistance is observed to be of the order of MΩ in the HRS vs kΩ in LRS. (b) Schematic representation of the bipolar switching in the memory element. With the device initially stayed in an equipotential state (the virgin state) with uniformly distributed oxygen vacancies prior to any electrical bias, a positive bias ($V_{Activation}$) is applied to create an electric potential gradient in order to induce ionic drift of the oxygen vacancies. After this irreversible electroforming process, a negative bias is applied to return the device from the LRS to HRS. Following the interface-type switching mechanism, the positively charged oxygen vacancies can be pushed toward (SET) and away from (RESET) the interface through a conduit that covers the entire junction size, respectively, by the positive and negative sweep biases. (c) Typical $I-V$ switching loop observed (without any evidence of negative differential resistance) in normal SET (OFF to ON) and RESET (ON to OFF) operations after the first activation/initialization process. For each measurement, the bias is applied on the top electrode, while the bottom electrode is grounded.

inset). To "activate" the device for the first time from its virgin state to the ON state, the applied bias is increased in small increments to generate an electric field gradient just sufficient to enable ionic drift (electromigration of oxygen vacancies in our case) between the top and bottom electrodes (Figure 2b). In the positive sweep (starting from zero applied voltage), the $I-V$ characteristic changes dramatically from the exponential

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behavior (of the virgin state, Figure 2a, inset) at +1.5 V. At this voltage, the device, for the first time, undergoes a sharp transition from the high resistance state (HRS) to the low resistance state (LRS) with a significant increase in the corresponding current (Figure 2a, top panel). Once activated, the corresponding $I-V$ profile of the device shows a symmetrical Ohmic behavior until −0.92 V during the negative sweep. At −0.92 V, the device exhibits a voltage-controlled negative differential resistance over a small range (from −0.92 V to −1.08 V) before it returns to the OFF state (i.e., the device undergoes a reverse transition from LRS to HRS) at the negative threshold (−1.5 V). This could correspond to the inhomogeneity in the electric field arising from scattered oxygen vacancies during the negative sweep. Because of this inhomogeneity, the interface could provide oxygen vacancy trapping sites created by electric field localization in the ultrananocrystalline film, which causes the difference in oxygen vacancy diffusion capacity and leads to the self-organized spatial pattern formation of the electric field domains[24] and to interface-type (isothermal) switching.[26] In a schematic representation of the complete switching mechanism (Figure 2b), the junction activation from the virgin state (i.e., first switching from the OFF to ON state) is followed by initialization (from the ON to OFF state), after which the device can be used in subsequent SET/RESET cycles during normal operation. During activation (the first positive sweep), a conduit made up of oxygen vacancies within the TiO_x matrix is formed to enable the ionic drift, and at this stage, some oxygen vacancies are permanently trapped at the bottom TiO_x/Pt interface. In the first negative sweep (the initialization step), the oxygen vacancies are driven away from the bottom electrode, which opens up a small gap between the trapped vacancies at the bottom electrode and the vacancies attracted toward the top electrode in the conduit (referred here as the conduit gap, Figure 2b). Because of the single-phase TiO_x film, this switching behavior is irrespective of the directional bias, i.e., the $I-V$ curve obtained with bias applied on the top electrode (and the bottom electrode grounded) is a mirror image of that obtained with the bias applied on the bottom electrode (and the top electrode grounded) (Figure S-5). This is an important result because almost all of the memristive devices reported to date are unidirectional,[8,25] where one of the interfaces is Ohmic with the other Schottky by default. This unidirectional switching characteristic is due to the presence of an additional TiO_2 layer in their device architecture,[4,5] which imposes the filament-type switching mechanism based on Joule heating. As the oxygen vacancies have to cross the insulating TiO_2 barrier by forming a filament (or filaments) via a tunneling process, a significantly higher applied bias is required. In our case, the Schottky and Ohmic interfaces are created with the ionic drift in the single-phase oxygen-deficient TiO_x layer, which removes the need for tunneling. This in turn enables the activation of the device at a much lower voltage and the device to be operated in a bidirectional fashion.

The corresponding $|I|$ vs V profiles (Figure 2a, middle panel) and resistance profile (Figure 2a, bottom panel) for the activation step illustrate the significant resistance difference between the HRS (∼MΩ) and LRS (∼kΩ). The latter also confirms the Schottky to Ohmic Pt/TiO_x interface exchange during the electric field induced ionic drift in the activation process. In contrast to the thermal dominated Chua's memristor,[1] where a critical temperature (induced by Joule heating) is required for filament formation, our memristor shows an extremely sharp transition between the HRS and LRS. This is because the low activation voltage (1.5 V) achieved in our case minimizes any excess heat such that the vacancy drift could occur at a temperature much lower than the critical temperature. This lower temperature freezes the resistance state, which induces a sharp transition between the HRS and LRS, illustrating the fast switching capability. This is a significant result because this activation voltage in our case is much smaller when compared to the majority of the electroforming voltages in earlier studies (6−10 V).[6,48−51] Even with the so-called electroforming-free devices, their switching (SET) voltages are reported to be 4 V,[52] 5 V,[45] and 10 V,[50] which are at least 6 times the SET voltage of the present device (0.59 V). Further, the strongly nonlinear and linear $I-V$ curves for the respective OFF and ON states provide much better sensitivity during the READ operation, where an almost constant ON-to-OFF current ratio can be achieved irrespective of the READ voltage. We attribute this to the increase of the localized electric field density as a result of the ultrananocrystalline nature of our TiO_x film and to the inherently high concentration of built-in oxygen vacancies, which reduce the need for further oxygen vacancy evolution at high bias through Joule heating.

Once activated, the device switching can then be described as transitions between two dynamic states (the ON and OFF states) enabled by two processes (SET and RESET). Starting with the OFF state, the device encounters high resistance, and it therefore provides a very small rectifying current. During the SET process, the device undergoes transition from the HRS (i.e., the OFF state) to LRS (i.e., the ON state), at which the device enters a conducting state that follows the Ohmic behavior. During RESET, the memristive device switches back from the LRS (ON state) to HRS (OFF state), and the device does not return to its virgin state ever again. Carrier transport is disturbed only up to a small extent by creating a conduit gap (Figure 2b). In the subsequent SET/RESET cycles, the device requires a smaller voltage sweep range than the activation voltage to extend and retract the conduit again for switching to the ON state and OFF state, respectively. For a typical Pt/TiO_x/Pt memristor, the SET and RESET can be repeated within ±1.0 V or less in the subsequent sweep cycles (Figure 2c). We also observe an important dependence of this SET/RESET voltage on the junction size, which is demonstrated in the following section. In the presence of the defect-rich TiO_x matrix, the resistive switching in our case is also found to be independent of the temperature of the working environment, which we have confirmed by changing the surrounding of the device, such as by covering the entire junction with an insulating polymer layer to prevent any heat dissipation during measurements, and by measuring the $I-V$ curve with the device immersed in liquid nitrogen. We observe no difference in the switching behavior in all three cases. This supports the interface-type switching model in our case, with no evidence for Joule heating based switching.

Size-Dependent Switching, Endurance, and Retention. The bipolar resistive behavior observed for our defect-rich ultrananocrystalline TiO_x based memristive devices indicates an interface-type switching mechanism, in which ionic drift is driven by electric field through the spatially formed conduit.[4,25,53] This is markedly different from the popular switching mechanism in TiO_x based memristive devices reported to date, which involves conducting filament formation within the oxide matrix along with unipolar characteristics

(unlike the bipolar switching that usually occurs in heterojunction devices).[5,54,55] The thermally driven filament-type and bias-driven interface-type resistive switching mechanisms can be differentiated by considering the area dependence of the current density for different junction sizes (50 × 50 μm^2, 20 × 20 μm^2, 10 × 10 μm^2, and 5 × 5 μm^2). The LRS-to-HRS current ratio is observed to be dependent on the area of the junction (Figure 3a). These results indicate that resistive switching in the Pt/TiO_x/Pt devices involves the entire junction area of the cell, i.e., the entire interface itself. This size dependence is also consistent with the smaller amounts of oxygen vacancies expected in smaller junctions. We also observe the direct effect of the junction size on the SET voltage, where the smaller is the junction size, the smaller are the SET voltage and current. This is illustrated in Figure 3a (inset) by the upward trend of the SET voltage and downward trends of the HRS and LRS resistances at 0.5 V with increasing junction size. Among the four junction sizes studied here, the smallest SET voltage (along with the smallest ON current) is observed to be +0.59 V for the 5 × 5 μm^2 junction size. As the typical filament size is a few tens of nanometer,[56−58] filament formation does not depend on the junction size, and conducting-filament-based switching is therefore junction-size independent. This is clearly not the case for our devices here. Our fabrication technique therefore promises excellent scalability for these devices, and we believe that even smaller SET voltages along with smaller ON currents can be obtained when the junction size is reduced to the nanoscale regime, which promises high-density integration of memristors with low power consumption.

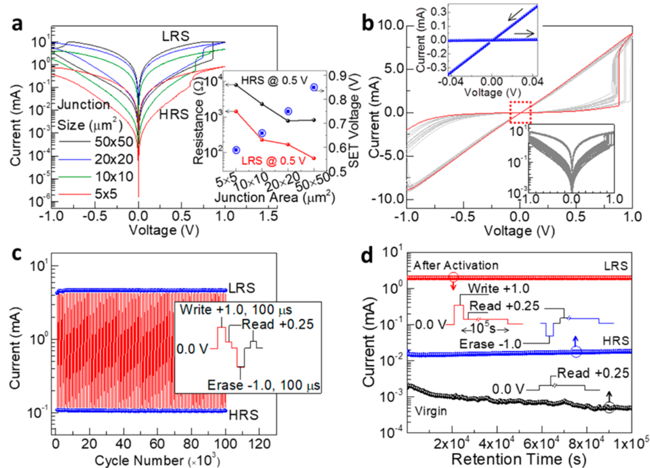

Figure 3. Junction size dependency, resistive switching endurance, and resistance state retention. (a) |*I*| vs *V* profiles of memristive devices with four different junction sizes (50 × 50 μm^2, 20 × 20 μm^2, 10 × 10 μm^2, and 5 × 5 μm^2) after the activation step. Lower currents are observed for devices with smaller junction sizes, and nearly similar LRS-to-HRS current ratios are found for all four junction sizes, which supports the interface-type memristive switching mechanism. The junction size has a direct effect on the current and SET voltage, which are nearly proportional to the junction size. Among the four junction sizes, the lowest SET voltage (+0.59 V) is obtained with the 5 × 5 μm^2 junction. The lower currents with smaller SET voltages thus obtained promise lower power consumption as the device miniaturization continues. This is also particularly promising for high-density device integration involving discrete SET and RESET processes. The inset compares device resistances of the HRS and LRS and the SET voltages observed for the four different junction sizes. (b) *I*−*V* curves and corresponding |*I*| vs *V* profiles (bottom inset) within the sweep voltage range of ±1.0 V for over 250 consecutive SET/RESET cycles for the memristive device with a 20 × 20 μm^2 junction size. The top inset shows that the device can be read even with a READ voltage as small as 40 mV. (c) ON and OFF currents obtained at a small READ voltage of +0.25 V for the 10^5 switching cycles, with the WRITE operation performed at V_{SET} = +1.0 V for 100 μs and the ERASE operation at V_{RESET} = −1.0 V for 100 μs. The currents for both the LRS and HRS are observed to be very stable throughout the sweep cycles. (d) Current vs time plots to illustrate the retention characteristics of the memristive device observed in LRS and HRS at a constant READ voltage of +0.25 V (WRITE at +1.0 V) after activation, in comparison with the current observed in the virgin state at the same READ voltage. The current obtained after the activation is extremely stable for over 10^5 s, with a projected device lifetime to be well over 10 years. For each measurement, the bias is applied on the top electrode, while the bottom electrode is grounded.

As shown by the nearly overlapping *I*−*V* profiles of over 250 consecutive switching cycles in Figure 3b, our Pt/TiO_x/Pt memristive devices also exhibit a high level of durability in terms of its switching repeatability. Each switching cycle is clearly marked by its sharp transition between the HRS and LRS, and the process is extremely reversible. The resistance of the HRS and LRS can be READ at a small voltage, which does not affect the resistance state. It is important to note that due to the Ohmic (linear) behavior of the ON state, the resistance remains the same in the LRS (throughout the bias range), which enables the use of a READ voltage as small as 40 mV (Figure 3b, top inset). The high-order endurance testing for over 10^5 cycles is performed by cycling a series of fast SET/RESET voltage pulses (with SET or WRITE voltage at +1.0 V for 100 μs and RESET or ERASE voltage at −1.0 V for 100 μs) and then sampling the current at a READ voltage of +0.25 V every 1000 cycles. The minimal power requirement for switching (i.e., writing and erasing) and reading operations makes the device highly desirable for building environment-friendly ultralow power consumption systems. The retention characteristic of a memristive device can be evaluated by monitoring the degradation in the current at a particular READ voltage applied for an extended period of time (Figure 3d). At a READ voltage of +0.25 V, the current obtained for the ON state is remarkably stable for over 10^5 s (with less than 1% variation in the average current of 2.0 mA), especially when compared to that in the OFF state (with ∼10% variation), which can be extrapolated to an estimated device lifetime of well over 10 years. The cumulative probability distribution plots of the resistance levels of the HRS and LRS (Figure S-6) show extremely narrow distributions, which suggest the exceptional uniformity of the resistance states of the device.

Device Response to Digital Signals. In analogy to the biological synapse, our device can be triggered between the LRS and HRS with READ voltage pulses applied for 0.5 s with a repetition interval of 5.5 s (Figure 4a) while reading the HRS at a successive smaller READ voltage of 0.05 V. The LRS current is observed to maintain a constant value for the duration and then rapidly return to its HRS value. Such very short response time and potentially fast switching speed are characteristic of excellent short-term potentiation (that can potentially be reduced to the nanosecond or shorter regime). This would enable the device to serve as a key building block in advanced computer logic circuits and potentially in neuromorphic circuits. Further experiments are required to demonstrate the potentiation model.[39] The device is also capable of maintaining its current values in the LRS and HRS

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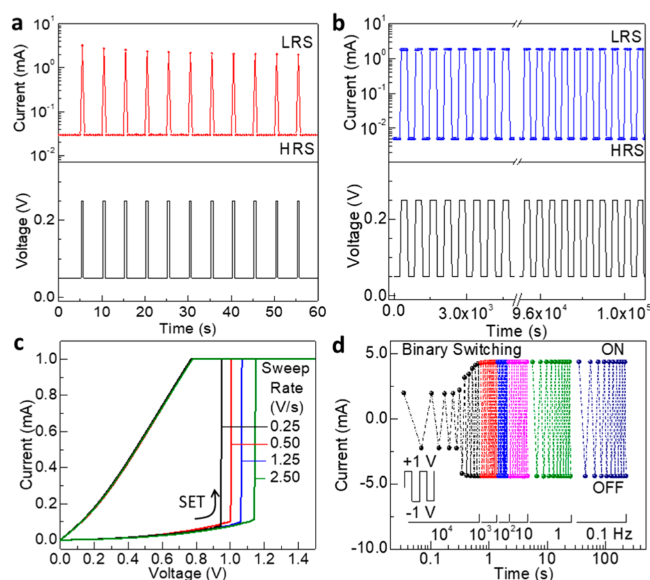

Figure 4. Memristor response to electric pulses with short and long time widths. (a) Resistive switching of the Pt/TiO_x/Pt device depicting stable current response upon short-term potentiation obtained with short electric pulses of +0.25 V amplitude (READ voltage) applied for 0.5 s in a 5.5 s interval at a READ voltage of 0.05 V. (b) The corresponding current response upon long-term potentiation obtained with stable LRS and HRS for READ voltage (set at +0.25 V) applied for 300 s in a 600 s interval over a testing period of 10^5 s. (c) SET voltages of the Pt/TiO_x/Pt device obtained at different sweep rates. V_{SET} tends to become smaller almost linearly with decreasing sweep rate. (d) Binary ON−OFF operation with alternating +1.0 V and −1.0 V pulses at different switching frequencies (10^4, 10^3, 10, 10, 1, 0.1 Hz) and corresponding pulse durations(100 μs, 1 ms, 10 ms, 100 ms, 1 s, and 10 s). Switching between the ON and OFF states is found to be independent of the input parameters, where the SET/RESET window is stable for all frequencies. For each measurement, the bias is applied on the top electrode, while the bottom electrode is grounded.

for an extended testing period of over 10^5 s, with repeated cycling of applying the respective read voltages of +0.25 V to observe LRS and a successive smaller read voltage of +0.05 V to observe HRS for a longer interval duration of 600 s (Figure 4b), which demonstrates the outstanding long-term potentiation of the device. This dual potentiation behavior of the device facilitates greater flexibility in achieving quick switching response at sequential LRS and HRS cycles with a set of small READ voltages. Upon further analysis of the switching behavior of this memristive device based on different sweep rates, V_{SET} is found to be highly dependent on and nearly proportional to the sweep rate, with smaller V_{SET} obtained for smaller sweep rates and vice versa (Figure 4c). When the voltage sweep rate is reduced, there is more time for the oxygen vacancies to drift toward the other interface, therefore reducing V_{SET}. When alternating electrical pulses of +1.0 V and −1.0 V are applied for different time periods (i.e., at different frequencies), the SET/RESET window (corresponding to the difference in current between the ON and OFF states) shows no obvious change in the ON-to-OFF current ratio with the switching frequency during the binary switching (Figure 4d). The ON-state and OFF-state currents are found to be extremely stable at all of the frequencies studied here (i.e., 10^4 Hz−0.1 Hz). This indicates that our memristive device is inherently more compatible with voltage switching at any frequency, which is in good accord with the electric field dominating interface-type switching.

■ CONCLUSION

In conclusion, we have successfully introduced a new ultrananocrystalline TiO_x material for fabricating low-bias-activated Pt/TiO_x/Pt (single-active-layer) memristive devices. Combined with the ultrananocrystalline nature (with an average crystallite size below 5 nm), the built-in oxygen vacancies in the defect-rich TiO_x matrix are found to be responsible for the electric field localization that enables oxygen vacancy trapping at discrete grain locations. This makes possible activation of the memory element at a much lower activation voltage (+1.5 V) than those reported in the literature, with the SET voltage as low as +0.59 V. Our bipolar devices follow the interface-type switching mechanism, consistent with the observed proportional current dependency on the junction size. High endurance for a large number of repeated cycles and high retention capacity of the device provide an estimated device lifetime of well over 10 years. Along with the low operating voltages and the resulting low power consumption advantage, the short-term and long-term potentiations at much smaller READ voltages make these devices potentially suitable for neuromorphic systems. The simple, completely room-temperature fabrication procedure for these high-performance memristive devices promises low-cost, scalable manufacturing of the next-generation ReRAM devices that can be easily integrable into a 3D stacking device architecture.

■ MATERIALS AND METHODS

Device Fabrication. The memristive devices were fabricated as a crossbar structure on a SiO_2/Si substrate by using a three-layer photolithographical procedure with a maskless photolithography system (SF-100 Xpress, Intelligent Micro Patterning Inc.). The device fabrication steps are schematically shown in Figure S-1a. Shipley 1805 photoresist (MicroChem) was spin-coated on the substrate, and the pattern was written under exposure of UV light (434 nm). The thickness of the photoresist layer was kept at 500 nm in order to achieve high-resolution features. A 500 nm thick layer of MCC primer (MicroChem) was spin-coated on the substrate before depositing the photoresist. Spin-coating parameters for the primer and photoresist layers were set to 4500 rpm for 40 s, and both layers were baked after the deposition on a hot plate set at 90 °C for 90 s. After the UV lithographical step with a 1.10 s exposure time, the written pattern was developed in a MF-24 developer (MicroChem) for 30 s and then rinsed with filtered high-resistivity water (resistivity ~18.2 MΩ). For the bottom electrode, a 5 nm thick Ti layer was predeposited as an adhesion layer before being sputter-deposited on a 60 nm thick Pt layer at room temperature, followed by the lift-off process. For the middle active layer, a high-purity TiO_x layer (60 nm thick) was produced via reactive sputtering at room temperature by in situ oxidation of Ti deposited by using a magnetron sputtering source from a Ti metal target (99.95% purity, ACI Alloys) in a high vacuum physical vapor deposition system (Mantis Deposition Ltd.), followed by the lift-off process. The Ar-flow was kept at 20 sccm to maintain the pressure of the deposition chamber (with a base pressure of 1×10^{-8} mbar) at 7.5×10^{-3} mbar. The TiO_x was formed by reactive sputtering in an oxygen-deficient environment. As the vacuum of the chamber used for the deposition was in the 10^{-4}−10^{-8} mbar range, the presence of residual ambient gas provided the source of oxygen. There was no external oxygen gas introduced into the deposition chamber to enable complete oxidation. A quartz crystal microbalance was used to monitor the thickness of the TiO_x film. Finally, a 30 nm thick Pt layer was deposited as the top electrode, following the same procedure used for the bottom electrode but for a shorter deposition time. All of the layer thicknesses were confirmed by using a profilometer (KLA Tencor P6).

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For physical characterization, we deposited, in separate experiments, TiO_x films on SiO_2/Si, Pt-coated SiO_2/Si, and glass substrates using the same parameters as those used for the actual devices. All of the substrates used in this work were cleaned ultrasonically in HPLC grade acetone, isopropyl alcohol, and filtered high-resistivity water. The SiO_2 layers (50 nm thick) were grown on Si substrates by annealing in an oxygen atmosphere in a quartz tube furnace, with oxygen flow rate set to 50 sccm and the temperature set to 900 °C for 90 min.

Characterization. The device morphology was characterized by field emission scanning electron microscopy (SEM) in a Zeiss Merlin electron microscope. Secondary ion mass spectroscopy (SIMS) was used to analyze the elemental composition of the fabricated devices in depth-profiling mode in an ION-TOF SIMS 5 system. The crystalline structures of the as-deposited and annealed TiO_x films were determined by using a PANalytical MRD X'pert Pro X-ray diffractometer with a Cu Kα X-ray source. UV−visible spectroscopy on the as-deposited and annealed TiO_x films was performed in a PerkinElmer Lambda 1050 spectrophotometer. For the electrical characterization studies, the resistive switching behavior of the fabricated devices was analyzed in I−V sweep mode with a two-probe DC measurement configuration by using an Agilent B1500 semiconductor analyzer coupled with an electrical probing station (Signatone Series 1160). Tungsten probe tips with a 10 μm tip size were used for connecting to the electrodes.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.7b07971.

Device fabrication and electron microscopic analysis, XPS analysis of the Pt/TiO_x/Pt memristor, SIMS depth profiles for the Pt/TiO_x/Pt memristor with a junction size of 50 × 50 μm^2, optical properties of as-deposited TiO_x film and upon annealing at 600 °C, virgin and activation states of the memristor devices with a 50 × 50 μm^2 junction size, cumulative probability distributions of resistance states, and table for comparison of various memristor architectures with single layer and multilayer switching matrices (PDF)

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Notes

The authors declare no competing financial interest.

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