Nanoscale

PAPER

Cite this: *Nanoscale*, 2019, **11**, 18159

Programmable, electroforming-free TiO_x/TaO_x heterojunction-based non-volatile memory devices†

Saurabh Srivastava, Joseph Palathinkal Thomas and Kam Tong Leung *

Electroforming-free resistive switching in memristors is essential to reliably achieving the performance of high switching speed, high endurance, good signal retention, and low power consumption expected for next-generation computing devices. Although there have been various approaches to resolve the issues observed with the electroforming process in oxide-based memory devices, most of them end up having high SET and RESET voltages and short lifetimes. We present a heterojunction interface of oxygen-vacancy-defect-rich ultrananocrystalline TiO_x and TaO_x films used as the switching matrix, which enables high-quality electroforming-free switching with a much lower programming voltage (+0.5–0.8 V), a high endurance of over 10^4 cycles and good retention performance with an estimated device lifetime of over 10 years. The electroforming-free switching behavior is governed by migration of oxygen vacancies driven by electric field localization that is imposed by the ultrananocrystalline nature of the TaO_x film, serving as the switching matrix, with the TiO_x film serving as an additional oxygen vacancy source to reduce the overall resistivity of TaO_x and provide low-bias rectification. The ability to perform electroforming-free resistive switching along with excellent switching repeatability and retention capabilities for various digital and analog programmable voltages enables high scalability and large density integration of the cross-bar ReRAM framework.

Received 26th July 2019,
Accepted 14th September 2019

DOI: 10.1039/c9nr06403f

rsc.li/nanoscale

Introduction

Memristors are becoming one of the pillars of the aspiring futuristic nanoelectronic industry, and they are expected to be soon used as a fundamentally new class of non-volatile memory devices in adaptive electronics such as neuromorphic circuits and artificial biological systems. Low power consumption, fast switching speed, and high endurance and retention performance are the basic requirements of any future non-volatile memory devices.[1–11] However, the irreversible electroforming step in the activation of the memristor remains one of the major obstacles to achieving high-density integration of this type of memory cell. In the past decade, filamentary switching[12–19] has been widely accepted as the switching mechanism in metal–oxide-based memristors. This mechanism involves the formation and rupture of a conducting filament (of an oxygen-deficient phase) in an insulating oxide matrix[20–22] between two metal electrodes, which is usually initiated by an electroforming voltage of ±6–10 V.[10,14,20,23] This electroforming process is required in order to create, in effect, an electric field sufficiently large to initiate a "soft" breakdown of the dielectric material. Such a breakdown process, however, does come with several notable disadvantages, including (a) time-consumption, because each device must undergo the electroforming step before commencing normal operation; (b) high variance among the devices and unreliable endurance, as the electroforming voltage could vary from sample to sample over a large number of devices on the same chip; and (c) low yield, because of the high probability of electroforming failure. All of these drawbacks are primarily caused by excessive Joule heating.[17,24–26] In addition, with potential further oxygen evolution in each cycle, the conducting channel could become damaged in each write–erase cycle, resulting in low reproducibility and short device lifetime. Electroforming-free switching of the memristor is therefore essential to facilitate reliable, non-destructive operation at low power with a long retention time and ultimately high-density integration.[20,27–30]

In contrast to filamentary switching, the less explored interface-type switching,[21,30–33] also known as vacancy modulating

WATLab and Department of Chemistry, University of Waterloo, 200 University Ave. W., Waterloo, Ontario N2L 3G1, Canada. E-mail: tong@uwaterloo.ca, saurabh@smart.mit.edu

†Electronic supplementary information (ESI) available: Additional SEM + EDX images of memristor arrays; XPS spectra of the C 1s and Pt 4f regions; AFM images of a typical TaO_x film; endurance data for multiple sweep cycles; and reproducibility of the devices; table of comparison of various devices reported in the literature and table of SET/RESET voltages with film thickness. See DOI: 10.1039/c9nr06403f

conductive oxide (VMCO) resistive switching, could offer an alternative mechanism for creating a stable electroforming-free memristor. These devices use electrical modulation of the defect profile to vary the conductance of the tunneling barrier. Recently, several research groups have begun to use nanostructure formation,[28] doping,[34] and multilayer stacking[35–38] in the switching matrix to create an electroforming-free memristor. These efforts remain largely limited by the high switching voltages (>4 V) and by the short lifetime (endurance) and retention capabilities. Here, we demonstrate the exceptional performance of a VMCO cell based on a novel hybrid TiO_x/TaO_x switching matrix that does not require electroforming.

With only the insulating Ta_2O_5 phase being the well-established equilibrium phase and multiple conducting phases (including TaO and TaO_x),[39] tantalum oxide is a well-known high-κ dielectric material commonly used in field-effect transistors,[40–42] and it is attracting a lot of interest for its use in memristor technology.[4,5,7,23,43,44] During the resistive switching of Ta_2O_5 based memristors, the insulating Ta_2O_5 phase transforms into the conducting TaO_x phase with the formation of oxygen vacancies initiated by Joule heating at a high applied bias.[1,38] However, even with some improvement in stability, their performance remains limited by the requirement of the irreversible electroforming process in its virgin state (prior to the normal switching between the SET and RESET states).

As each layer could play a significant role in the switching mechanism, heterojunction devices have been adopted as an important class of device architecture for memristors.[10,29,45–48] We present a memristive switching device based on, for the first time, the TiO_x/TaO_x heterojunction. In this device, TaO_x in its metastable state serves as the reservoir for the oxygen vacancies, while the switching occurs in the TiO_x layer. The first switching in this device is observed to occur at a much smaller voltage of +0.8 V compared to previously reported devices (see Table S-1† for better comparison).[1,20,38,49] With the subsequent 10^4 switching cycles also performed at similarly low voltages, this device exhibits high performance found in the top such devices reported in the literature. We further show that the switching behavior of the device can be controlled by careful optimization of the volume of the switching matrix (*e.g.* by varying the thickness of the active layer). We also demonstrate that once the heterojunction interface of the switching matrix is activated, the SET/RESET voltages can be tuned by programming the *I*–*V* measurement parameters such as the compliance current, stopping voltage, and width of the bias voltage pulse.

Results and discussion

Fabrication and characterization of the Pt/TiO_x/TaO_x/Pt device architecture

In our recent work,[3] we develop a single-layer TiO_x based memristor that exhibits interface-type switching activated by a low bias. The nanocrystalline nature of the oxygen-deficient TiO_x layer enables excellent endurance and retention capabilities in our device with much smaller SET/RESET voltages than those of the majority of devices reported in the literature. In the present work, we build a new memristor device capable of operating not only entirely electroforming-free but also at a low bias (Fig. S-1†). This is made possible by introducing a heterojunction multilayer device architecture with the addition of a tantalum oxide film in order to provide in-built oxygen vacancies. As the crucial material for the top electrode (TE) and bottom electrode (BE) for obtaining stable memory cells, Pt is chosen because of its work function, with the Fermi level in a near-perfect match with the defect states of TaO_x. Our heterojunction memristor therefore has three different interfaces: Pt/TiO_x (top), TiO_x/TaO_x (middle) and TaO_x/Pt (bottom), each of which plays a significant role in the overall resistive switching event. A typical heterojunction crossbar device structure, fabricated on a SiO_2/Si substrate, is shown schematically in Fig. 1a. The area of the active matrix layer, *i.e.* the TiO_x/TaO_x layer, sandwiched between the top and bottom Pt electrodes defines the junction size or cell size. The thickness of the TiO_x film is kept constant at 10 nm, while four different thicknesses (10, 20, 40 and 60 nm) of the TaO_x film, obtained by employing appropriate deposition times, are used. Fig. S-1a and S-1b† show the SEM images and corresponding EDX maps of the devices, while Fig. 1b shows the cross-sectional TEM image of the memristor device with a junction size of 10 × 10 μm^2, along with the cross-sectional TEM-EDX maps (Fig. 1b, inset). The top Pt layer appears slightly thinner than the bottom Pt layer, which is due to sample preparation used for the cross-sectional TEM analysis. The corresponding high-resolution TEM images of the TaO_x, TiO_x and Pt regions shown in Fig. 1c clearly indicate the nanocrystalline nature of all three films (with ultrasmall crystallite sizes <4 nm).

The glancing-incidence X-ray diffraction patterns for TaO_x films (separately deposited over a large area on Pt-coated SiO_2/Si substrates) with different film thicknesses are shown in Fig. 1d. The predominant XRD features of the 10 nm thick TaO_x film correspond only to the underlying nanocrystalline Pt film, with a crystallite size of 4–5 nm (as estimated by the Scherrer analysis). Appearing as shoulders of the nearby Pt features, the TaO_x (220) and other features are found to be considerably weaker, which suggests that the 10 nm thick TaO_x film is largely amorphous. All other thicker TaO_x films exhibit sharper and more well-defined TaO_x features with increasing film thickness, all with a nanocrystallite size less than 2–3 nm. The nanocrystalline structure in the thicker TaO_x films is likely induced by the underlying Pt layer, which provides the template for the nanocrystalline growth with a longer deposition time. Depth-profiling XPS analysis has been performed on the 60 nm thick TaO_x film deposited on a Pt-coated SiO_2/Si substrate. The Ta 4f spectrum for the as-deposited film (Fig. 1e) shows an intense Ta $4f_{7/2}$ ($4f_{5/2}$) peak at 27.0 (28.9) eV and a weaker Ta $4f_{7/2}$ ($4f_{5/2}$) feature at 22.3 (24.2) eV, corresponding to Ta_2O_5 and TaO_x ($1 \leq x \leq 3$), respectively,[20,50] the former of which is likely due to surface oxidation in air. Upon sputtering for 30–60 s, the Ta_2O_5 feature is evidently reduced, while the

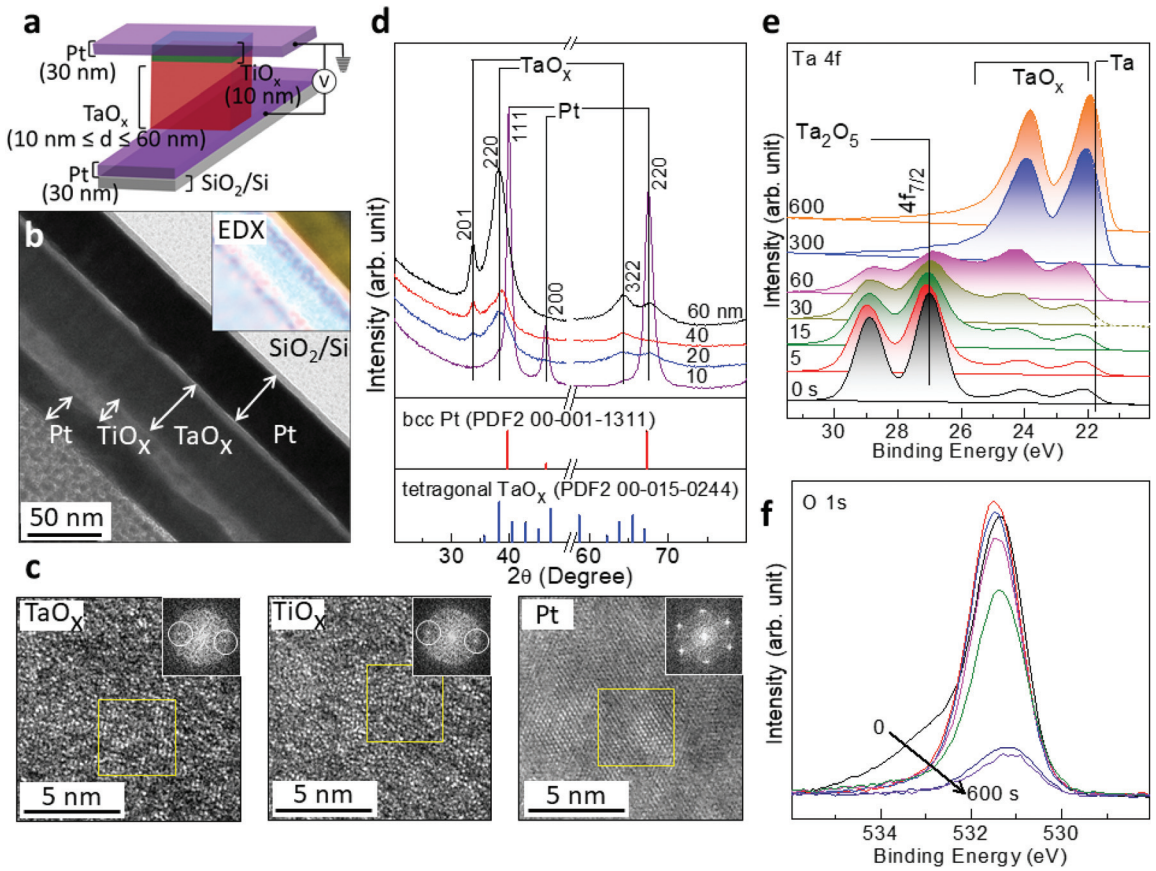

Fig. 1 Device structure and physical characterization of the Pt/TiO_x/TaO_x/Pt heterojunction. (a) Schematic diagram of the multilayer architecture of the Pt/TiO_x/TaO_x/Pt memristor device. The TiO_x layer thickness is kept the same at 10 nm, while the TaO_x layer thickness is varied from 10 to 60 nm in order to observe the effect of the TaO_x layer thickness on the electrical behavior of the memristor device. (b) Cross-sectional TEM image and the corresponding EDX elemental maps of the device (inset) [color coding: blue for Pt, red for TiO_x and green for TaO_x]. (c) High-resolution TEM images of the corresponding nanocrystalline TaO_x, TiO_x and Pt regions (insets show FFT images of the selected area in the corresponding TEM images). (d) XRD patterns of TaO_x films with four different thicknesses (10, 20, 40 and 60 nm), each deposited on a 60 nm thick Pt layer supported on a SiO_2/Si substrate, along with the reference patterns for tetragonal TaO_x (PDF2 00-015-0244) and bcc Pt (PDF2 00-001-1311). (e and f) Depth profiling XPS spectra of the Ta 4f and O 1s regions for the 60 nm thick TaO_x film deposited on a 60 nm thick Pt layer (*i.e.*, without the top Pt/TiO_x layers), supported on a SiO_2/Si substrate.

oxygen-deficient TaO_x layer appears to increase in intensity.[50] The TaO_x peaks become quite intense upon sputtering to 300 s. After 600 s of sputtering, TaO_x appears to undergo ion-induced reduction to metallic Ta with the Ta $4f_{7/2}$ ($4f_{5/2}$) feature at 21.8 (23.8) eV.[51,52] The corresponding intensity change in the O 1s feature at 531.5 eV is consistent with the initial removal of surface Ta_2O_5 in the first 60 s of sputtering, followed by the more steady O 1s intensity after reaching the TaO_x layer upon sputtering for 300 s (Fig. 1f). The corresponding depth-profiling C 1s and Pt 4f spectra are shown in Fig. S-2.† The R_{RMS} surface roughness of the oxide film obtained from AFM analysis is found to be 0.84 nm for a 5 × 5 μm^2 scan area (Fig. S-3†).

Memristor performance and switching mechanism

In its virgin state (prior to the application of any electrical bias), the Pt (TE)/TiO_x/TaO_x/Pt (BE) device remains in a high resistance state (HRS) (~MΩ), consistent with the oxygen vacancies uniformly distributed in the bulk of the TaO_x film.[17,53] As an intrinsic Schottky-like barrier exists between the Pt BE and TaO_x layer, the device exhibits an exponential current–voltage behavior. The resistance of the device in the virgin state can be determined by measuring the current (I) as a function of the small applied voltage (V).

The resistance state can be tuned by applying a positive bias voltage on the Pt BE, with the Pt TE grounded, to create a sufficiently large electric field to drive these positively charged oxygen vacancies from one electrode to another. Resistive switching in the TiO_x/TaO_x heterojunction memristor can therefore be understood in terms of drift of the in-built oxygen vacancies (cationic ion transport) from the BE to the TE in the TaO_x layer followed by diffusion of these oxygen vacancies into the more electronegative TiO_x layer (relative to TaO_x).[20] Such a process is often known as valence change memory.[6] In the present case, electroforming-free resistive switching is achieved because at the TiO_x/TaO_x heterojunction, the more electronegative system TiO_x with δ^- charge tends to attract the cations (containing the oxygen vacancies) while the electrons

are being attracted towards $TaO_x^{\delta+}$ even at a low bias. The leakage current (the HRS current level at low voltage) remains very low because of the high-κ dielectric nature of the TaO_x layer. The process in which the device goes from the HRS to the low resistance state (LRS) is called SET, with the corresponding voltage V_{SET}. Similarly, RESET is the reverse process when the device goes from the LRS to the HRS with the voltage V_{RESET}.

A typical *I–V* curve for switching the TiO_x/TaO_x heterojunction device is shown in both linear and semilog scales in Fig. 2a. The resistance of the device changes from the HRS (low current region) to the LRS (high current region) at V_{SET} (+0.8 V), *i.e.* from the distinct binary state 0 (OFF) to the binary state 1 (ON), when a positive sweep voltage is applied on the TaO_x/Pt interface (BE) side (with the TE grounded). During the reverse sweep, the device follows the ohmic characteristic until V_{RESET} (−2.0 V), at which the device returns to the HRS. An exponential *I–V* behavior is observed from V_{RESET} to V_{SET} (forward sweep), while a linear *I–V* behavior is found from V_{SET} to V_{RESET} (reverse sweep). The resistive switching from the HRS to the LRS at low V_{SET}, as demonstrated in the present heterojunction device, is highly desirable for the low-power-consumption, high-performance CMOS technology. To demonstrate the importance of these novel heterojunction devices in achieving electroforming-free switching behavior, we compare the present results with those obtained with just one active layer, *i.e.* a 60 nm TaO_x film, sandwiched between the top and bottom Pt electrodes. In a separate experiment, we fabricate such a Pt/TaO_x/Pt memristor device (*i.e.* without the TiO_x layer and with all the other parameters the same). Evidently, the corresponding *I–V* curve (Fig. 2b) shows that there is no clear switching onset from the HRS to the LRS, over the same sweep range of ±2.0 V, in marked contrast to the Pt/TiO_x/TaO_x/Pt memristor that exhibits discrete ON and OFF states with V_{SET} at +0.8 V and V_{RESET} at −2.0 V.

The electric field dominating switching mechanism of our heterojunction devices is supported by the dependence of the resistive switching behavior on the junction size. We have fabricated our TiO_x/TaO_x heterojunction devices with four different junction sizes. The corresponding current density *vs.*

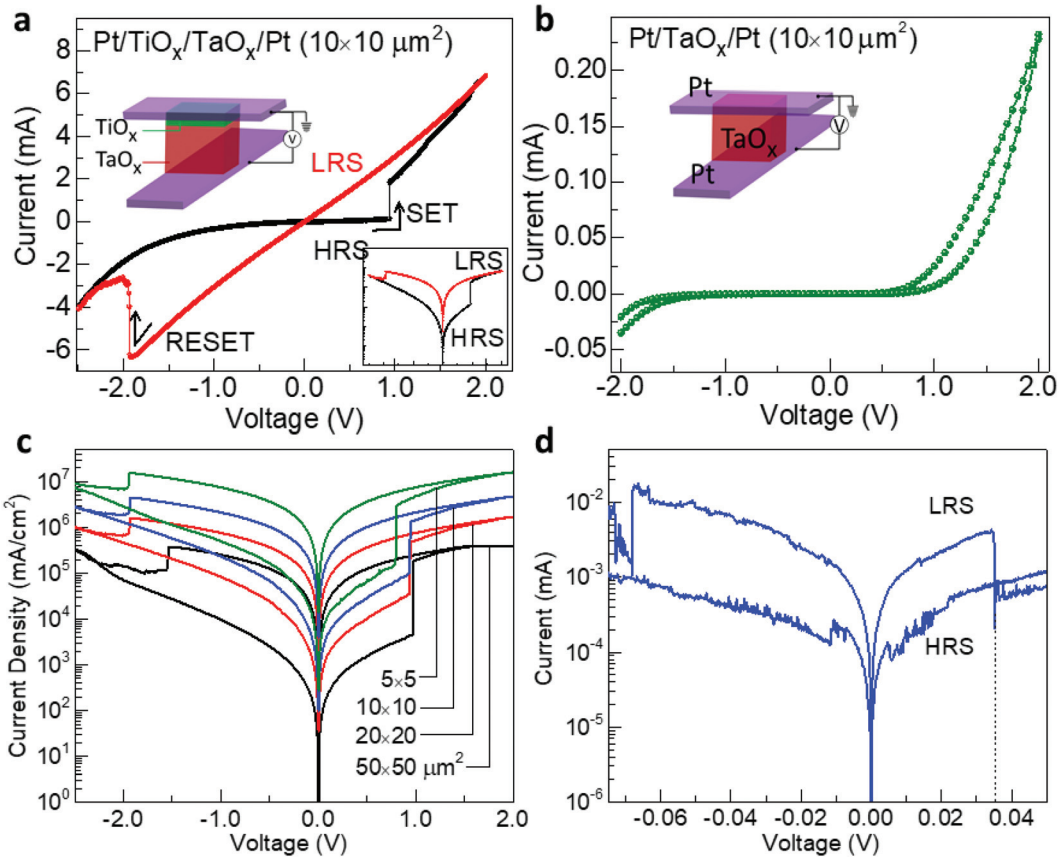

Fig. 2 Switching characteristics of a TiO_x/TaO_x based memory cell. (a) *I–V* curve and log|*I*| *vs.* *V* curve (inset) of the Pt/TiO_x/TaO_x/Pt memristor with a 10 × 10 μm^2 junction size exhibiting bipolar resistive switching, where the SET process switches the device from the HRS (OFF) to the LRS (ON) while the RESET process switches the LRS back to the HRS. (b) *I–V* curve of a Pt/TaO_x/Pt memristor with the same dimensions as the Pt/TiO_x/TaO_x/Pt memristor but without the TiO_x layer. (c) Log|*J*| *vs.* *V* curves obtained for the Pt/TiO_x/TaO_x/Pt memristors with four different junction sizes (5 × 5 μm^2, 10 × 10 μm^2, 20 × 20 μm^2, 50 × 50 μm^2) illustrating the junction size effect with very similar switching (SET) voltages. (d) Log|*I*| *vs.* *V* curve of the device shown in (a) to illustrate its low power (300 nW) performance achieved for an ultra-low programming voltage of <50 mV with an ON current of ~10 μA.

voltage (J–V) curves (Fig. 2c) of all four junction sizes provide clear evidence of their junction size dependence, where the smaller junction size exhibits the larger (better) ON-to-OFF current density ratio at almost the same V_{SET}. This is because as the dimension of the junction area becomes smaller, the oxygen vacancies are more constricted to flow directly (between the BE and TE) by the same applied electric field (due to a higher electric field density). We also show that by setting a smaller compliance current (~10 μA in our case) our device is observed to be switched with a much smaller programming voltage (V_{SET} < 50 mV) and the LRS current is in the μA range (Fig. 2d). Fig. S-4a† shows the LRS current *vs.* voltage for the device at different compliance currents where the LRS current is found to be decreasing with smaller compliance current. This behavior shows the potential of multistage switching in our devices.

Fig. 3 shows a schematic diagram for the proposed switching mechanism based on the movement of oxygen vacancies. These oxygen vacancies are uniformly distributed in both TiO_x and TaO_x films in its virgin state (Fig. 3a) while the TiO_x/TaO_x and Pt (TE)/TiO_x interfaces remain in the HRS. When a positive voltage is applied to the Pt BE, the oxygen vacancies in the TaO_x film drift towards the Pt TE under the generated electric field. Below V_{SET}, however, the field is not strong enough for the vacancies to diffuse through the TiO_x layer to switch the device into the LRS (Fig. 3b and c). With further increase in the applied V_{SET} to above a threshold value, these vacancies make their way through the TiO_x layer and reach the Pt TE layer while the oxygen vacancies in the TiO_x layer also travel toward the TE under the generated field. In this SET process, tunneling and diffusion of oxygen vacancies occur and the vacancies could be pushed easily towards the Pt TE, thereby switching the device to the LRS (Fig. 3d). In the reverse sweep, the oxygen vacancies are pushed away from the top electrode and the device goes back to the HRS. In this RESET process, a no-vacancy zone in the TiO_x layer is created[54] (Fig. 3e). After the first cycle, the SET and RESET processes could be repeated by applying a similar set of V_{SET} and V_{RESET} voltages.

While investigating the effect of the TaO_x film thickness on the resistive switching performance of our Pt/TiO_x/TaO_x/Pt heterojunction device with a 10 × 10 μm^2 junction, we observe that the switching voltage for TaO_x films thinner than 10 nm is more than twice that of the thicker films. This switching behavior could be correlated with the crystalline nature of the films with different film thicknesses where a 10 nm thick TaO_x film is largely amorphous while thicker TaO_x films are largely nanocrystalline (Fig. 1d). Unlike the other thicker nanocrystalline TaO_x films that undergo switching below +0.8 V, the device with the 10 nm thick amorphous TaO_x film does not switch and it does not undergo the SET process until V_{SET} is +1.7 V. In the negative sweep, the RESET process is achieved when V_{RESET} is more negative than −2.5 V. This behavior could be caused by the depletion of conductive defects such as metallic Ta or oxygen vacancies in the amorphous TaO_x films, in accord with the structural non-homogeneity in the amorphous film. The ON and OFF currents for devices with

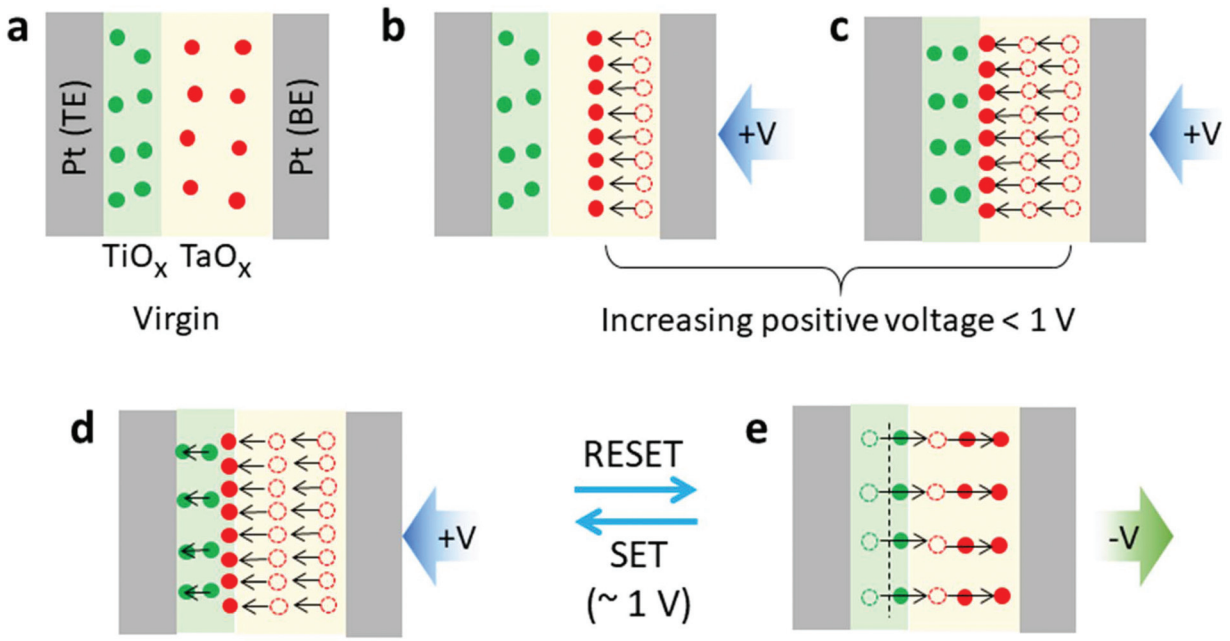

Fig. 3 Schematic diagram of various states of the switching cycle for a Pt/TiO_x/TaO_x/Pt heterojunction memristor. (a) Virgin state under zero bias conditions, where the oxygen vacancies in TiO_x (green solid dots) and TaO_x (red solid dots) are distributed randomly inside the respective layers. (b and c) Oxygen vacancies in TaO_x begin to drift towards TiO_x upon applying a positive voltage V_{SET} (below a threshold value) at the bottom electrode (BE) with the top electrode (TE) grounded. (d) When V_{SET} reaches a sufficiently high value, the oxygen vacancies can easily migrate to the TE, and the device switches into the LRS. (e) When the voltage is swept back to V_{RESET}, the oxygen vacancies are pushed away from the TE side and the device switches back to the HRS.

different TaO_x film thicknesses are compared in Fig. 4b. Although the 10 nm TaO_x film shows a higher ON/OFF current ratio, the devices with a 60 nm thick TaO_x film and a 10 × 10 μm^2 junction size are found to have the best ON-to-OFF current ratio (among all devices reported in the present work) when the SET voltages (being much lower) are taken into con-

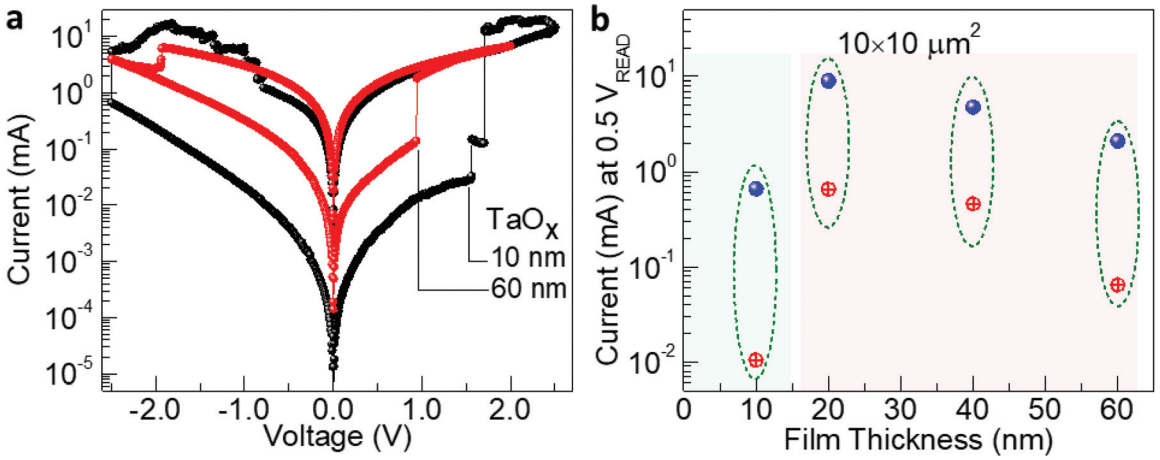

Fig. 4 Effects of TaO_x film thickness in the TiO_x/TaO_x memristors with a 10 × 10 μm^2 junction size on SET and RESET. (a) Resistive switching for memristors with 10 nm and 60 nm thick TaO_x layers. (b) The corresponding currents obtained at +0.5 V applied bias for the HRS (OFF) (red spheres) and the LRS (ON) (blue spheres) of memristors with different TaO_x film thicknesses.

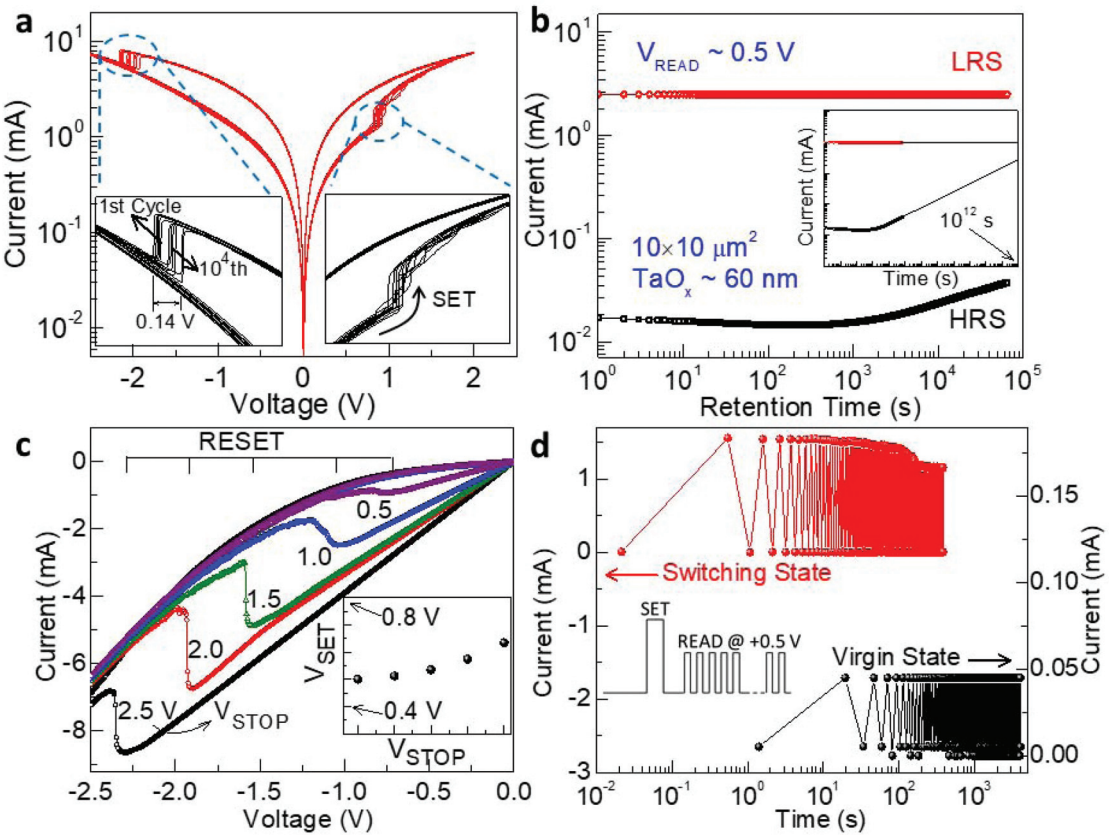

Fig. 5 Endurance, retention capabilities, and programmable switching modes of the TiO_x/TaO_x memristor with a 10 × 10 μm^2 junction size and a TaO_x film thickness of 60 nm. (a) Log|*I*| *vs.* *V* curves of over 10^4 cycles with expanded views of selected regions shown in the insets. (b) Currents obtained at a READ voltage of 0.5 V for the HRS and LRS for over 10^5 s, illustrating the high retention capabilities of the device. Linear extrapolation of the retention data projects the device lifetime to be over 10 years (inset). (c) RESET for different stopping voltages V_{STOP} (+0.5 to +2.5 V) with the corresponding SET voltages V_{SET} shown in the inset. SET and RESET can be manually programmed by using different stopping voltages. (d) Uniform resistance variation with repeated electrical cycles for READ pulses of +0.5 V with a pulse interval of 0.5 s before and after the device has gone through the first SET process at 1.0 V.

sideration. These devices are used to further evaluate their device stability and endurance.

We show, in Fig. 5a, the remarkable repeatability and endurance in the *I–V* profiles of our memristor device with a $10 \times 10\ \mu m^2$ junction size and a 60 nm thick TaO_x film for over 10 000 cycles (following the first switching cycle), all with similar V_{SET} and V_{RESET}. As the repeated cycling between the HRS and LRS does not involve the formation of additional oxygen vacancies and consequently corrosion due to Joule heating, there is therefore no detectable degradation of the device behavior. There is also no discernible difference between V_{SET} for the first switching cycle from the HRS to the LRS and those for the subsequent cycles, which confirms that a high-bias electroforming step is not required to initiate the device operation. Furthermore, the device is found to maintain similar ON and OFF currents up to 10^5 s at a READ voltage of +0.5 V (Fig. 5b). This indicates the high retention capacity of our heterojunction memristive device, as one of the best among other reported devices.[1,36,45,55–60] There is a small increase in the HRS current (Fig. 5b) that corresponds to the slow and constant formation of oxygen vacancies within the small voltage regime over a period of time. Fig. S-4† shows the retention characteristics of the devices for different read voltages, and the read-out current in the LRS is found to be very stable after the long retention. Linear extrapolation of the data provides the estimated lifetime of the devices to be more than 10 years (inset of Fig. 5b). We also fabricate over 300 memristor devices, each with a junction size of $10 \times 10\ \mu m^2$, on the same chip (Fig. S-5†). All these devices exhibit essentially the same switching voltage V_{SET}, which demonstrates the high reproducibility and robustness of our fabrication process.

To program or tune the SET and RESET voltages of the device, the stopping voltage (the maximum positive voltage during the *I–V* sweep) is found to play an important role. Evidently, V_{RESET} becomes smaller with decreasing stopping voltage during the SET process (Fig. 5c). The SET voltage is also found to decrease in a similar fashion (Fig. 5c inset) but the change is small when compared to that found for the RESET voltage (Table S-2†). This is an important result for the integration of programmable circuits, because the behavior of the device can be programmed by simply setting the stopping voltage. In addition to the analog switching characteristics demonstrated above, uniform resistance variations with repeated electrical cycles in the virgin state and in the switching state are observed at a READ voltage of +0.5 V when applying DC electrical pulses of ±1.0 V on the device. The interval between the electrical pulses is set to be 0.5 s. Evidently, a stable ON-to-OFF current ratio is obtained in both the virgin state and the switching state, as shown in Fig. 5d. This memristive behavior is interesting because it has been suggested that such a behavior is similar to the behavior of synaptic connections between neurons that can be made stronger or weaker through polarity, strength and duration of the chemical or electrical signals.[10]

Conclusion

Using a TiO_x/TaO_x heterostructure-based materials system, we have successfully fabricated an electroforming-free non-volatile memory device with a remarkably low programing voltage (+0.5 V) and other notable device performances (such as endurance up to 10^4 cycles and retention up to 10^5 s). The nanocrystalline, oxygen vacancy-rich TaO_x layer in our memristor device is found to enable the bipolar interface-type switching mechanism. By stacking a high-κ dielectric material such as TaO_x with a more electronegative TiO_x layer, we produce a hybrid active matrix for an excellent memory device with much smaller SET voltages, extremely high repeatability/endurance and stable ON-to-OFF current ratios. Our study on the effects of different junction sizes and TaO_x layer thicknesses on the switching behavior of the devices further shows that these device structural parameters can be used to control the switching voltage and the ON-to-OFF current ratios. More importantly, the programmable switching behavior under both analog and pulsed signals makes these memristor devices potential candidates for advanced logic components for computers and adaptive circuits. This study paves the way to develop quantitative models to understand other device architectures based on hybrid materials and to further exploit the benefits of continued miniaturization by creating even smaller junctions using advanced nanoscale lithography techniques.

Materials and methods

Device fabrication

A maskless optical lithography system (Intelligent Micropatterning Inc.) was used to fabricate crossbar memristors on SiO_2/Si substrates through three-layer photolithographical steps (Fig. S-1†). Shipley 1827 photoresist (MicroChem) was spin-coated (at 3500 rpm for 40 s) onto the substrate, followed by baking at 90 °C on a hot plate for 60 s. Photolithography was then performed under the exposure of UV light (434 nm). The written pattern was developed in an MF-24 developer (MicroChem) for 60 s followed by rinsing with filtered high-resistivity (18.2 MΩ) water. For the bottom electrode, a 30 nm thick Pt layer was sputter-deposited on the SiO_2/Si substrate at room temperature in an I bar configuration followed by a lift-off process. For the middle active-matrix layer, a high purity TaO_x layer (60 nm thick) was deposited at room temperature using radio frequency (RF) magnetron sputtering of a Ta metal target (99.95% purity, ACI Alloys) in a physical vapor deposition system (Mantis Deposition Ltd) with a base pressure of 1×10^{-8} mbar, followed by RF sputter-deposition of a high-purity TiO_x (10 nm thick) layer from a Ti target and then by a lift-off process. Finally, the Pt top electrode was deposited in an I bar configuration oriented perpendicular to the bottom electrode using the same procedure as that for the bottom electrode. The film thicknesses of all the layers were determined by using a profilometer (KLA Tencor P6). For

physical characterization, the TiO_x layer and the top electrode were not deposited, and the TaO_x films were deposited on Pt-coated SiO_2/Si substrates using the same parameters as those used for the actual devices. Prior to the photolithography steps, all the Si substrates used in the present work were sequentially cleaned ultrasonically in HPLC-grade acetone, isopropyl alcohol, and filtered high-resistivity water. The SiO_2/Si substrates used for the aforementioned photolithography steps were obtained by annealing Si substrates in an oxygen atmosphere in a quartz tube furnace for 90 min and the resulting native oxide layer was estimated to be ~100 nm thick.

Characterization

The surface morphology and crystallinity of the metal and metal oxide films of different film thicknesses in our memristor device were characterized by transmission electron microscopy (TEM) using a Zeiss Libra 200MC microscope, field-emission scanning electron microscopy (SEM) using a Zeiss Merlin electron microscope, and glancing-incidence X-ray diffraction (XRD) using a PANalytical X'pert Pro MRD diffractometer with a Cu Kα X-ray source. An Bruker energy-dispersive X-ray (EDX) analysis system coupled with the TEM system was used for elemental mapping. The cross-sectional TEM samples (lamella) were prepared using a Zeiss Auriga focused ion beam SEM system. In order to characterize the chemical-state compositions of the layers in the fabricated devices, X-ray photoelectron spectroscopy (XPS) was conducted in the depth-profiling mode using a Thermo-VG Scientific ESCALab 250 microprobe equipped with a monochromatic Al Kα X-ray source (1486.6 eV). Argon ion sputtering was performed over a raster area of 3 × 3 mm^2 at an ion beam energy of 3 keV and a typical sample current density of 110 nA mm^{-2}. The XPS data were fitted using the CasaXPS software after removing the Shirley background. For the electrical characterization studies, the resistive switching behavior of the fabricated devices was measured in the *I–V* sweep mode using a Signatone Series 1160 DC measurement system coupled to an Agilent B1500 semiconductor analyzer. Tungsten probe tips with a 10 μm tip size were used for connecting to the electrodes. All the *I–V* measurements were performed at room temperature.

Conflicts of interest

The authors declare no competing financial interest.

Acknowledgements

This work was supported by the Natural Sciences and Engineering Research Council (NSERC) of Canada.

References

1 M. J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y. B. Kim, C. J. Kim, D. H. Seo, S. Seo, *et al.*, A Fast, High-Endurance and Scalable Non-Volatile Memory Device Made from Asymmetric Ta_2O_{5-x}/TaO_{2-x} Bilayer Structures, *Nat. Mater.*, 2011, **10**, 625–630.

2 K. J. Yoon, M. H. Lee, G. H. Kim, S. J. Song, J. Y. Seok, S. Han, J. H. Yoon, K. M. Kim and C. S. Hwang, Memristive Tri-Stable Resistive Switching at Ruptured Conducting Filaments of a Pt/TiO_2/Pt Cell, *Nanotechnology*, 2012, **23**, 185202.

3 S. Srivastava, J. P. Thomas, N. F. Heinig and K. T. Leung, High-Performance Single-Active-Layer Memristor Based on an Ultrananocrystalline Oxygen-Deficient TiO_x Film, *ACS Appl. Mater. Interfaces*, 2017, **9**, 36989–36996.

4 A. Wedig, M. Luebben, M. Moors, D. Y. Cho, K. Skaja, T. Hasegawa, K. K. Adepalli, B. Yildiz, R. Waser and I. Valov, Nanoscale Cation Motion in TaO_x, HfO_x and TiO_x Memristive Systems, *Nat. Nanotechnol.*, 2015, **11**, 67–75.

5 F. Miao, W. Yi, I. Goldfarb, J. J. Yang, M. X. Zhang, M. D. Pickett, J. P. Strachan, G. Medeiros-Ribeiro and R. S. Williams, Continuous Electrical Tuning of the Chemical Composition of TaO_x-Based Memristors, *ACS Nano*, 2012, **6**, 2312–2318.

6 R. Waser, R. Dittmann, G. Staikov and K. Szot, Redox-Based Resistive Switching Memories - Nanoionic Mechanisms, Prospects, and Challenges, *Adv. Mater.*, 2009, **21**, 2632–2663.

7 J. J. Yang, M. X. Zhang, J. P. Strachan, F. Miao, M. D. Pickett, R. D. Kelley, G. Medeiros-Ribeiro and R. S. Williams, High Switching Endurance in TaO_x Memristive Devices, *Appl. Phys. Lett.*, 2010, **97**, 232102.

8 D. B. Strukov, G. S. Snider, D. R. Stewart and R. S. Williams, The Missing Memristor Found, *Nature*, 2008, **453**, 80–83.

9 L. O. Chua, Memristor-The Missing Circuit Element, *IEEE Trans. Circuit Theory*, 1971, **18**, 507–519.

10 Y.-F. Wang, Y.-C. Lin, I.-T. Wang, T.-P. Lin and T.-H. Hou, Characterization and Modeling of Nonfilamentary Ta/TaO_x/TiO_2/Ti Analog Synaptic Device, *Sci. Rep.*, 2015, **5**, 10150.

11 A. C. Torrezan, J. P. Strachan, G. Medeiros-Ribeiro and R. S. Williams, Sub-Nanosecond Switching of a Tantalum Oxide Memristor, *Nanotechnology*, 2011, **22**, 485203.

12 A. Chung, J. Deen, J. S. Lee and M. Meyyappan, Nanoscale Memory Devices, *Nanotechnology*, 2010, **21**, 412001.

13 C. Lee, I. Kim, H. Shin, S. Kim and J. Cho, Nonvolatile Memory Properties of Pt Nanoparticle-Embedded TiO_2 Nanocomposite Multilayers via Electrostatic Layer-by-Layer Assembly, *Nanotechnology*, 2010, **21**, 185704.

14 H. Jiang and Q. Xia, Effect of Voltage Polarity and Amplitude on Electroforming of TiO_2 Based Memristive Devices, *Nanoscale*, 2013, **5**, 3257–3261.

15 U. Celano, L. Goux, A. Belmonte, K. Opsomer, A. Franquet, A. Schulze, C. Detavernier, O. Richard, H. Bender, M. Jurczak, *et al.*, Three-Dimensional Observation of the Conductive Filament in Nanoscaled Resistive Memory Devices, *Nano Lett.*, 2014, **14**, 2401–2406.

16 C. N. Lau, D. R. Stewart, R. S. Williams and M. Bockrath, Direct Observation of Nanoscale Switching Centers in

Metal/Molecule/Metal Structures, *Nano Lett.*, 2004, **4**, 569–572.
17 D. H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X. S. Li, G. S. Park, B. Lee, S. Han, *et al.*, Atomic Structure of Conducting Nanofilaments in TiO_2 Resistive Switching Memory, *Nat. Nanotechnol.*, 2010, **5**, 148–153.
18 S. Kumar, C. E. Graves, J. P. Strachan, E. M. Grafals, A. L. D. Kilcoyne, T. Tyliszczak, J. N. Weker, Y. Nishi and R. S. Williams, Direct Observation of Localized Radial Oxygen Migration in Functioning Tantalum Oxide Memristors, *Adv. Mater.*, 2016, **28**, 2772–2776.
19 C. Lenser, A. Koehl, I. Slipukhina, H. Du, M. Patt, V. Feyer, C. M. Schneider, M. Lezaic, R. Waser and R. Dittmann, Formation and Movement of Cationic Defects during Forming and Resistive Switching in $SrTiO_3$ Thin Film Devices, *Adv. Funct. Mater.*, 2015, **25**, 6360–6368.
20 J. H. Yoon, S. J. Song, I. H. Yoo, J. Y. Seok, K. J. Yoon, D. E. Kwon, T. H. Park and C. S. Hwang, Highly Uniform, Electroforming-Free, and Self-Rectifying Resistive Memory in the $Pt/Ta_2O_5/HfO_{2-x}/TiN$ Structure, *Adv. Funct. Mater.*, 2014, **24**, 5086–5095.
21 J. J. Yang, J. Borghetti, D. Murphy, D. R. Stewart and R. S. Williams, A Family of Electronically Reconfigurable Nanodevices, *Adv. Mater.*, 2009, **21**, 3754–3758.
22 D. Y. Cho, M. Luebben, S. Wiefels, K. S. Lee and I. Valov, Interfacial Metal-Oxide Interactions in Resistive Switching Memories, *ACS Appl. Mater. Interfaces*, 2017, **9**, 19287–19295.
23 J. P. Strachan, G. Medeiros-ribeiro, J. J. Yang, M.-X. Zhang, F. Miao, I. Goldfarb, M. Holt, V. Rose and R. S. Williams, Spectromicroscopy of Tantalum Oxide Memristors, *Appl. Phys. Lett.*, 2011, **98**, 242114.
24 A. A. Sharma, M. Noman, M. Abdelmoula, M. Skowronski and J. A. Bain, Electronic Instabilities Leading to Electroformation of Binary Metal Oxide-Based Resistive Switches, *Adv. Funct. Mater.*, 2014, **24**, 5522–5529.
25 D. Panda, F. M. Simanjuntak and T.-Y. Tseng, Temperature Induced Complementary Switching in Titanium Oxide Resistive Random Access Memory, *AIP Adv.*, 2016, **6**, 075314.
26 A. S. Alexandrov, A. M. Bratkovsky, B. Bridle, S. E. Savel'ev, D. B. Strukov and R. Stanley Williams, Current-Controlled Negative Differential Resistance Due to Joule Heating in TiO_2, *Appl. Phys. Lett.*, 2011, **99**, 202104.
27 J. P. Strachan, J. J. Yang, L. A. Montoro, C. A. Ospina, A. J. Ramirez, A. L. D. Kilcoyne, G. Medeiros-Ribeiro and R. S. Williams, Characterization of Electroforming-Free Titanium Dioxide Memristors, *Beilstein J. Nanotechnol.*, 2013, **4**, 467–473.
28 S. Lee, A. Sangle, P. Lu, A. Chen, W. Zhang, J. S. Lee, H. Wang, Q. Jia and J. L. Macmanus-driscoll, Novel Electroforming-Free Nanoscaffold Memristor with Very High Uniformity, Tunability, and Density, *Adv. Mater.*, 2014, **26**, 6284–6289.
29 C. T. Chou, B. Hudec, C. W. Hsu, W. L. Lai, C. C. Chang and T. H. Hou, Crossbar Array of Selector-Less TaO_x/TiO_2 Bilayer RRAM, *Microelectron. Reliab.*, 2015, **55**, 2220–2223.
30 L. Michalas, S. Stathopoulos, A. Khiat and T. Prodromakis, Conduction Mechanisms at Distinct Resistive Levels of $Pt/TiO_{2-x}/Pt$ Memristors, *Appl. Phys. Lett.*, 2018, **113**, 143503.
31 J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart and R. S. Williams, Memristive Switching Mechanism for Metal/Oxide/Metal Nanodevices, *Nat. Nanotechnol.*, 2008, **3**, 429–433.
32 U. Celano, C. Gastaldi, B. Govoreanu, O. Richard, H. Bender, L. Goux, G. S. Kar and W. Vandervorst, Evidences of Areal Switching in Vacancy-Modulated Conductive Oxide (VMCO) Memory, *Microelectron. Eng.*, 2017, **178**, 122–124.
33 S. Subhechha, B. Govoreanu, Y. Chen, S. Clima, K. De Meyer, J. Van Houdt and M. Jurczak, Extensive Reliability Investigation of A-VMCO Nonfilamentary RRAM: Relaxation, Retention and Key Differences to Filamentary Switching, in *IEEE International Reliability Physics Symposium Proceedings*, 2016, pp. 6C21–6C25.
34 S. Kim, S. Choi, J. Lee and W. D. Lu, Tuning Resistive Switching Characteristics of Tantalum Oxide Memristors through Si Doping, *ACS Nano*, 2014, **8**, 10262–10269.
35 Y. C. Bae, A. R. Lee, J. B. Lee, J. H. Koo, K. C. Kwon, J. G. Park, H. S. Im and J. P. Hong, Oxygen Ion Drift-Induced Complementary Resistive Switching in Homo $TiO_x/TiO_y/TiO_x$ and Hetero $TiO_x/TiON/TiO_x$ Triple Multilayer Frameworks, *Adv. Funct. Mater.*, 2012, **22**, 709–716.
36 A. A. Bessonov, M. N. Kirikova, D. I. Petukhov, M. Allen, T. Ryhänen and M. J. A. Bailey, Layered Memristive and Memcapacitive Switches for Printable Electronics, *Nat. Mater.*, 2015, **14**, 199–204.
37 A. Prakash, S. Maikap, H. C. Chiu, T. C. Tien and C. S. Lai, Enhanced Resistive Memory Characteristics and Switching Mechanism Using a Ti Nanolayer at the W/TaO_x Interface, *Nanoscale Res. Lett.*, 2014, **9**, 125.
38 Q. Zhou and J. Zhai, Resistive Switching Characteristics of $Pt/TaO_x/HfN_x$ Structure and Its Performance Improvement, *AIP Adv.*, 2013, **3**, 032102.
39 S. P. Garg, N. Krishnamurthy and A. Awasthi, The O-Ta (Oxygen-Tantalum) System, *J. Phase Equilib.*, 1996, **17**, 63–77.
40 C. T. Lee and Y. S. Chiu, Field-Effect-Transistor-Based Calcium Ion Sensors Using $Zn_3Ta_2O_5$ Sensing Membrane, *Sens. Actuators, B*, 2014, **203**, 790–794.
41 H. Zhu, J. E. Bonevich, H. Li, C. A. Richter, H. Yuan, O. Kirillov and Q. Li, Discrete Charge States in Nanowire Flash Memory with Multiple Ta_2O_5 Charge-Trapping Stacks, *Appl. Phys. Lett.*, 2014, **104**, 233504.
42 J. W. Liu, M. Y. Liao, M. Imura, E. Watanabe, H. Oosato and Y. Koide, Diamond Field Effect Transistors with a High-Dielectric Constant Ta_2O_5 as Gate Material, *J. Phys. D: Appl. Phys.*, 2014, **47**, 245102.
43 Y. Yang, P. Sheridan and W. Lu, Complementary Resistive Switching in Tantalum Oxide-Based Resistive Memory Devices, *Appl. Phys. Lett.*, 2012, **100**, 203112.

44 F. Gu, S. F. Wang, M. K. Lü, G. J. Zhou, D. Xu and D. R. Yuan, Photoluminescence Properties of SnO_2 Nanoparticles Synthesized by Sol–Gel Method, *J. Phys. Chem. B*, 2004, **108**, 8119–8123.

45 J. H. Yoon, S. Yoo, S. J. Song, K. J. Yoon, D. E. Kwon, Y. J. Kwon, T. H. Park, H. J. Kim, X. L. Shao, Y. Kim, *et al.*, Uniform Self-Rectifying Resistive Switching Behavior via Preformed Conducting Paths in a Vertical-Type Ta_2O_5/HfO_{2-x} Structure with a Sub-μm (2) Cell Area, *ACS Appl. Mater. Interfaces*, 2016, **8**, 18215–18221.

46 G. Wei, H. Murakami, T. Fujioka, A. Ohta, Y. Goto and S. Higashi, Microelectronic Engineering Impact of Insertion of Ultrathin TaO_x Layer at the Pt/TiO_2 Interface on Resistive Switching Characteristics O 1s, *Microelectron. Eng.*, 2011, **88**, 1152–1154.

47 Q. Lv, S. Wu, J. Lu, M. Yang, P. Hu and S. Li, Conducting Nanofilaments Formed by Oxygen Vacancy Migration in Ti/TiO_2/TiN/MgO Memristive Device, *J. Appl. Phys.*, 2011, **110**, 104511.

48 M. Hansen, M. Ziegler, L. Kolberg, R. Soni, S. Dirkmann, T. Mussenbrock and H. Kohlstedt, A Double Barrier Memristive Device, *Sci. Rep.*, 2015, **5**, 13573.

49 Y. Nishi, K. Fleck, U. Bottger, R. Waser and S. Menzel, Effect of RESET Voltage on Distribution of SET Switching Time of Bipolar Resistive Switching in a Tantalum Oxide Thin Film, *IEEE Trans. Electron Devices*, 2015, **62**, 1561–1567.

50 S. Srivastava, J. P. Thomas, N. F. Heinig, M. Abd-ellah, M. A. Rahman and K. T. Leung, Effcient Photoelectrochemical Water Splitting on Ultrasmall Defect-Rich TaO_x Nanoclusters Enhanced by Size-Selected Pt Nanocluster Promotors, *Nanoscale*, 2017, **9**, 14395–14404.

51 S. Hashimoto, C. Tanaka, A. Murata and T. Sakurada, Formulation for XPS Spectral Change of Oxides by Ar Ion Bombardment: Application of the Formulation to Ta_2O_5 System, *J. Surf. Anal.*, 2006, **13**, 14–18.

52 K. S. Park, D. Y. Lee, K. J. Kim and D. W. Moon, Growth and Characterization of Ta_2O_5 Thin Films on Si by Ion Beam Sputter Deposition, *Thin Solid Films*, 1996, **281–282**, 419–422.

53 H. Nili, S. Walia, S. Balendhran, D. B. Strukov, M. Bhaskaran and S. Sriram, Nanoscale Resistive Switching in Amorphous Perovskite Oxide (*a*-$SrTiO_3$) Memristors, *Adv. Funct. Mater.*, 2014, **24**, 6741–6750.

54 J. Lee, W. D. Lu and E. Kioupakis, Electronic and Optical Properties of Oxygen Vacancies in Amorphous Ta_2O_5 from First Principles, *Nanoscale*, 2017, **9**, 1120–1127.

55 H. Nili, S. Walia, A. E. Kandjani, R. Ramanathan, P. Gutruf, T. Ahmed, S. Balendhran, V. Bansal, D. B. Strukov, O. Kavehei, *et al.*, Donor-Induced Performance Tuning of Amorphous $SrTiO_3$ Memristive Nanodevices: Multistate Resistive Switching and Mechanical Tunability, *Adv. Funct. Mater.*, 2015, **25**, 3172–3182.

56 K. M. Kim, J. Zhang, C. Graves, J. J. Yang, B. J. Choi, C. S. Hwang, Z. Li and R. S. Williams, Low-Power, Self-Rectifying, and Forming-Free Memristor with an Asymmetric Programing Voltage for a High-Density Crossbar Application, *Nano Lett.*, 2016, **16**, 6724–6732.

57 S. Wu, L. Ren, J. Qing, F. Yu, K. Yang, M. Yang, Y. Wang, M. Meng, W. Zhou, X. Zhou, *et al.*, Bipolar Resistance Switching in Transparent ITO/$LaAlO_3$/$SrTiO_3$ Memristors, *ACS Appl. Mater. Interfaces*, 2014, **6**, 8575–8579.

58 C. Yoshida, K. Tsunoda, H. Noshiro and Y. Sugiyama, High Speed Resistive Switching in Pt/TiO_2/TiN Film for Nonvolatile Memory Application, *Appl. Phys. Lett.*, 2007, **91**, 223510.

59 A. Zaffora, D. Y. Cho, K. S. Lee, F. Di Quarto, R. Waser, M. Santamaria and I. Valov, Electrochemical Tantalum Oxide for Resistive Switching Memories, *Adv. Mater.*, 2017, **29**, 1–6.

60 C. Baeumer, R. Waser, R. Dittmann, S. Menzel, A. Marchewka, N. Bernier, C. La Torre, R. E. Dunin-Borkowski and D. Cooper, Anomalous Resistance Hysteresis in Oxide ReRAM: Oxygen Evolution and Reincorporation Revealed by In Situ TEM, *Adv. Mater.*, 2017, **29**, 1700212.

