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Induced Complementary Resistive Switching in Forming-Free TiO_x/TiO_2/TiO_x Memristors

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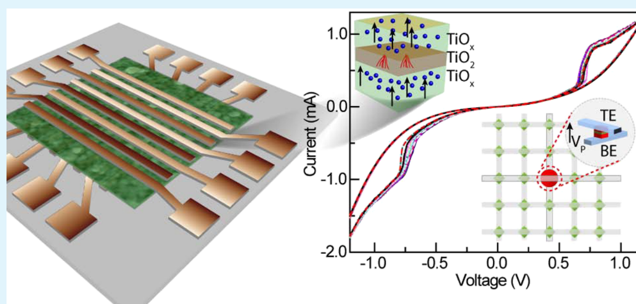

ABSTRACT: The undesirable sneak current path is one of the key challenges in high-density memory integration for the emerging cross-bar memristor arrays. This work demonstrates a new heterojunction design of oxide multilayer stacking with different oxygen vacancy contents to manipulate the oxidation state. We show that the bipolar resistive switching (BRS) behavior of the Pt/TiO_x/Pt cross-bar structure can be changed to complementary resistive switching (CRS) by introducing a thin TiO_2 layer in the middle of the TiO_x layer to obtain a Pt/TiO_x/TiO_2/TiO_x/Pt device architecture with a double-junction active matrix. In contrast to the BRS in a single-layer TiO_x matrix, the device with a double-junction matrix remains in a high-resistance state in the voltage range below the SET voltage, which makes it an efficient structure to overcome the sneak path constraints of undesired half-selected cells that lead to incorrect output reading. This architecture is capable of eliminating these half-selected cells between the nearby cross-bar cells in a smaller programming voltage range. A simplified model for the switching mechanism can be used to account for the observed high-quality switching performance with excellent endurance and current retention properties.

KEYWORDS: *Low power, electroforming-free memristor, sneak path elimination, cross-talk, TiO_x, complementary resistive switching*

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■ INTRODUCTION

Resistive random access memory (ReRAM) or a memristor is a potential candidate for future non-volatile memories that promise low-energy consumption and high scalabilities.[1−4] However, to incorporate them in adaptive circuits such as neuromorphic and artificial biological systems, improvement in the memristor properties, including power consumption, switching speed, and endurance/retention, requires more effort.[5−7] ReRAM is generally based on the valence change mechanism, in which switching between the high-resistance state (HRS) and low-resistance state (LRS) is affected by the migration of oxygen vacancies.[8−10] In this inherently bipolar switching mechanism, different bias polarities are required to toggle between the switching states. The first basic obstacle for these memories is the need for a high-bias electroforming voltage, which could alter the device structure due to excess heat generation and further oxygen evolution.[11] To mitigate the need for the required electroforming process, various approaches such as introducing in-built oxygen vacancies, hybrid nanostructures, and multilayer stacking have been attempted.[6,12−14] We have shown previously that by creating an ultrananocrystalline, highly oxygen-deficient switching matrix between a pair of metal electrodes, the electroforming voltage can be significantly reduced.[15] We further demonstrated that integrating two oxygen-deficient layers of materials with different electronegativity could produce electroforming-free memristors.[4] These memristors have been found to exhibit high READ and WRITE operation speeds and low power consumption with very high endurance. These properties should enable them to be integrated into cross-bar array structures and even in three-dimensional stacking architecture with a cell size of $4F^2/n$, where F is the minimum feature size and n is the number of layers.[8,16−19]

The high-density cross-bar structures built by integrating memristors (bidirectional memories), however, suffer from the second obstacle, that is, the cross-talk problem that results from the unintended multiple parallel sneak paths in the network, which could lead to misreading a designated cell within the passive cross-bar array without interference from the unselected low-resistance cells.[20−22] The high-density fabrication of a nano/microscale cross-bar array causes close proximity among the cells and increased possibility of cross-talk. This problem could limit the size of the array and also increase the power consumption due to undesired combined output. This issue can be resolved by adding diodes or

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transistors to the system as selector elements to make the memristors unidirectional.[23] Despite the use of such additional components to address the sneak path problem, complementary resistive switching (CRS) has attracted much interest as an elegant solution to reduce the sneak current in the cross-bar memory without using any external component.[24,25] The most common method of creating CRS is by introducing a metallic layer in the middle of the oxide layer or by combining two bipolar memristors anti-serially. Linn et al.[26] reported CRS in two anti-serially connected Pt/SiO_2/GeSe/Cu cross-bars, where CRS is achieved by toggling the resistance between the LRS and HRS at a voltage higher than the threshold voltage. Other reports have focused on achieving CRS using a double-layer switching matrix such as TiO_{2-x}/TiN_xO_y ($x/y > 3$),[27] ZrO_x/HfO_x,[28] or even a single-layer HfO_2.[29] The idea behind developing such structures is to suppress the *IV* characteristics of the device in a smaller bias range so that the neighboring cells are unaffected by a sneak current. This type of device exhibits two HRSs, where the binary information “0” and “1” is stored. In both of these states, only one of the cells is in the LRS while the other is in the HRS. The read margin calculations for bipolar resistive switching (BRS) and CRS devices show that the ON/OFF current ratio does not impact the achievable array size in the BRS architecture, while a significant increase in the array size could be achieved with a higher ON/OFF current ratio in the CRS system.[26,30,31] In the present work, we carefully tune the heterostructure to achieve CRS, while preserving the interface-type switching mechanism at a voltage higher than the threshold voltage to keep low-bias switching operation viable. Instead of preparing two memories anti-serially connected to each other, we constructed a single cross-bar structure by inserting a high-resistance TiO_2 layer in between two highly oxygen-deficient TiO_x layers sandwiched between two Pt electrodes, that is, the Pt/TiO_x/TiO_2/TiO_x/Pt ($x < 2$) device structure. The thin TiO_2 layer controls the complementary switching behavior by regulating the electromigration of oxygen vacancies between the two highly oxygen-deficient TiO_x layers that provide the low-bias switching. We also compare the results of unipolar CRS with BRS based on Pt/TiO_x/Pt device stacking and contrast their switching mechanisms. The new device also exhibits high-quality repeatability and endurance and good retention capabilities. The ability of our CRS memristor to stay in the HRS within a low voltage range resolves the prominent cross-talk problem between adjacent memory bits, which makes this structure an excellent candidate for highly interconnected memristor architectures.

RESULTS AND DISCUSSION

The cross-sectional transmission electron microscopy (TEM) images of the Pt/TiO_x/TiO_2/TiO_x/Pt double-junction device are shown in Figure 1a (Figure S1a of the Supporting Information shows the scanning electron microscopy (SEM) image of the 10 × 10 μm^2 cross-bar arrays). The high-resolution TEM images reveal the nanocrystalline nature of the double-junction TiO_x/TiO_2/TiO_x film. The corresponding X-ray diffraction (XRD) profiles in Figure S1b,c confirm the ultrananocrystalline nature of the TiO_x layer with a crystallite size of 3−4 nm (as estimated by the Scherrer analysis), which is consistent with the TEM images. The thin TiO_2 layer (2−3 nm) in the middle of two TiO_x layers could be observed in the cross-sectional TEM image. However, as the valence change from Ti^{4+} to Ti^{3+}/Ti^{2+} (corresponding to the change in oxygen

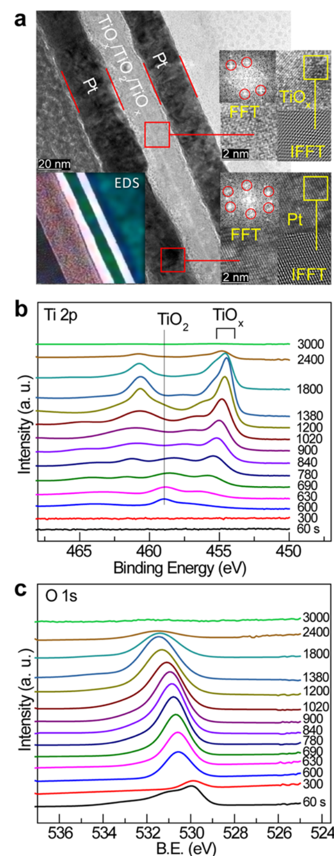

Figure 1. Physical characterization of double-junction devices. (a) Low-magnification cross-sectional TEM image and the corresponding energy-dispersive X-ray spectroscopy (EDS) elemental map (inset) of the Pt/TiO_x/TiO_2/TiO_x/Pt device, along with high-resolution TEM images and fast Fourier transform images of selected regions of the TiO_x/TiO_2/TiO_x and Pt layers. (b,c) XPS spectra of the respective Ti 2p and O 1s regions as the functions of Ar^+-sputtering time.

vacancies) does not have a significant effect on the lattices in the oxide layers,[32] it is, therefore, unlikely to crystallographically differentiate the ultrathin TiO_2 layer in the middle of the TiO_x layers. The X-ray photoelectron spectroscopy (XPS) spectra of Ti 2p, O 1s, and Pt 4f regions of the Pt/TiO_x/TiO_2/TiO_x/Pt device as functions of the Ar^+-sputtering time are shown in Figures 1b,c, and S2a, respectively. The respective chemical-state composition of each layer is verified from these three sets of XPS region spectra. The intensity of the Pt 4f feature of the top electrode layer starts to decrease after 690 s of sputtering (Figure S2a) as the Ti 2p peak at 454 eV emerges (Figure 1b), along with an increase in the O 1s intensity (Figure 1c), originating from the top Pt/TiO_x interface. Similarly, the peak intensity for Pt increases after 1800 s of sputtering with a reduction in the intensity of Ti 2p and O 1s peaks, which shows that sputtering has reached the bottom TiO_x/Pt interface. The binding energy of metallic Pt 4f appears to correspond well with the reported value of the Pt $4f_{7/2}$ peak (at 71.2 eV with Pt $4f_{5/2}$ at 74.5 eV, as marked by dashed lines in Figure 1b). The small shifts in binding energy of the Pt $4f_{7/2}$ peak from 71.2 eV and the O 1s peak from below 530 eV obtained after the initial sputtering for 60 s correspond to the removal of ambient induced surface hydrocarbons (as shown in the C 1s spectra in Figure S2b). Furthermore, the weak Ti^{4+} feature (with the Ti $2p_{3/2}$ peak at 459 eV) found upon sputtering for less than 690 s is due to

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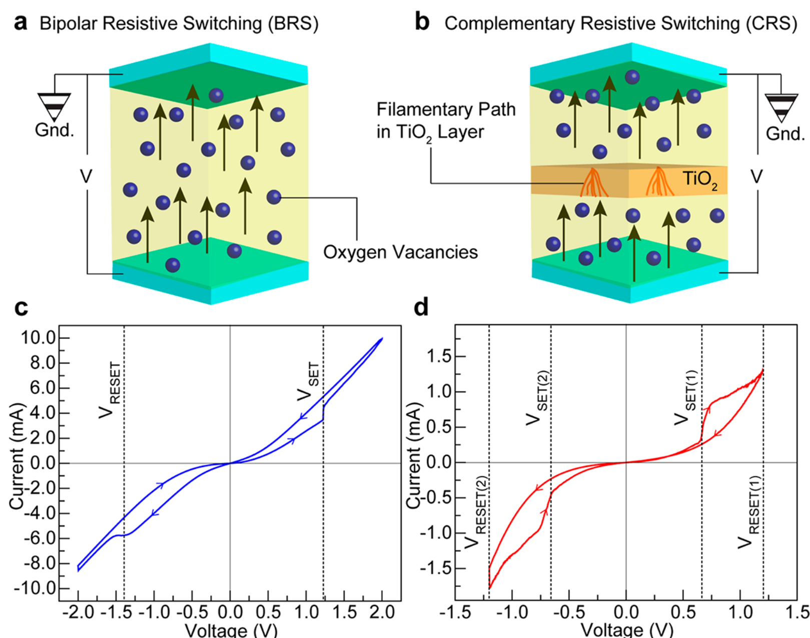

Figure 2. BRS and CRS. (a,b) Schematic representations and (c,d) current−voltage (or I−V) curves of (a,c) $Pt/TiO_x/Pt$ and (b,d) $Pt/TiO_x/TiO_2/TiO_x/Pt$ devices. The bipolar memristor consists of a single TiO_x layer sandwiched between two Pt layers ($Pt/TiO_x/Pt$), where the oxygen vacancies are pushed into or out of the metal/semiconductor interfaces by applying different voltage polarities to the bottom electrode (with the top electrode at ground). The complementary memristor is obtained by inserting a TiO_2 layer (a high-resistance layer) in the middle of the TiO_x layer to create a $Pt/TiO_x/TiO_2/TiO_x/Pt$ device structure. The BRS memristor device follows the interface-type bipolar switching where opposite voltage polarities are required to SET and RESET the device. The BRS device can be SET by applying a positive voltage to the bottom electrode in the forward sweep, whereas RESET is achieved by applying a negative voltage to the bottom electrode in the reverse sweep (both with the top electrode at ground). The CRS memristor can be SET and RESET by applying voltages with the same polarity with $|V_{SET(1)}| < |V_{RESET(1)}|$ in the forward sweep and $|V_{SET(2)}| < |V_{RESET(2)}|$ in the reverse sweep. The CRS device always stays in the HRS for $V_{SET(1)} > V > V_{SET(2)}$, thereby avoiding the cross-talk problem through sneak paths among neighboring devices.

ambient oxidation of TiO_x to TiO_2 outside the junctions and in areas not covered with the top Pt electrode. With increasing sputtering time from 690 to 1800 s, the Ti $2p_{3/2}$ peak location reduces to 455.6−454.4 eV, corresponding to a combination of Ti^{3+} and Ti^{2+} components in the bulk (from the junction points).[33,34] This evolution of peaks at different binding energies suggests an oxygen-deficiency gradient distribution. The O 1s feature at 530.5−531.5 eV (upon sputtering up to 300 s) also corresponds to the change from the Ti^{4+} phase to the Ti^{3+} and Ti^{2+} states, as represented by the TiO_x phase. With a sampling depth window of about 10 nm, it is difficult to catch the thin TiO_2 layer at exactly the right depth to reveal the changes in the depth-profiling XPS results.

The schematic configurations of both bipolar ($Pt/TiO_x/Pt$) and unipolar ($Pt/TiO_x/TiO_2/TiO_x/Pt$) memristors are depicted in Figure 2a,b, respectively. The corresponding IV curves exhibiting BRS, with one SET and one RESET, and CRS, with two SETs and two RESETs, are shown in Figure 2c,d. The BRS device ($Pt/TiO_x/Pt$) can be SET by applying a positive bias to the bottom electrode (with the top electrode at ground) in the forward sweep, following an interface-type switching behavior.[4,15] The device stays in the LRS until RESET in the reverse sweep, which requires a negative bias to the bottom electrode (with the top electrode at ground). As the device resistance that is responsible for switching correlates with the amount of Ti^{2+}, the composition of the oxidation states, therefore, plays a crucial role. On the other hand, the CRS device ($Pt/TiO_x/TiO_2/TiO_x/Pt$) can be SET, that is, switching from the HRS to the LRS, by applying a positive bias at $V_{SET(1)}$ and then RESET, that is, switching from the LRS back to the HRS, by further increasing the positive bias voltage to $V_{RESET(1)}$, all in the forward sweep. In the reverse sweep, the device switches from an HRS to an LRS at $V_{SET(2)}$ and back to the HRS at $V_{RESET(2)}$.

Figure 3 shows the resistive switching characteristics of the cross-bar memories with three different oxide matrices. According to the characteristic of BRS, the device is switched from the HRS to the LRS by applying a positive bias V_{SET} in the forward sweep.[15,32] The BRS device with the $Pt/TiO_x/Pt$ device architecture shows the high degree of switching repeatability with near-overlapping semilog IV profiles over 10^5 consecutive switching cycles (Figure 3a), within a voltage sweep range of −1.5 to +1.5 V (with the magnified plot shown in the inset). Figure S3a shows an excellent retention behavior of the BRS device for up to 10^6 s (at different V_{READ} values of +0.25, +0.5, and +1.0 V). The IV characteristic is independent of the bias sweeping direction because of the symmetrical structure of the device stacking. Here, our focus is on achieving the CRS behavior, while keeping the SET voltage of the device as low as possible. In contrast to the other CRS device architectures,[26,27,35] where two identical devices are anti-serially connected to each other from the same side of electrodes, our TiO_x-based BRS device is rebuilt as a CRS device by incorporating a thin TiO_2 layer in the middle of the TiO_x layer, as shown in Figure 3b (left inset). The middle TiO_2 layer in our CRS system works as a high-resistive barrier to maintain one of the junctions always in the HRS, and thus, the device remains inactive under low bias. The CRS event in this device structure is governed by a combination of both the interface-conducting path and filamentary switching. In this

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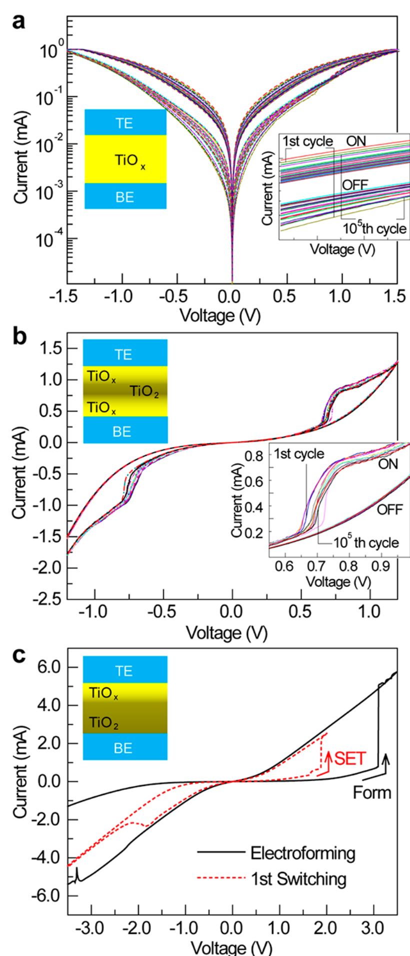

Figure 3. Endurance behavior of BRS and CRS devices. (a,b) *IV* plots within a sweeping range of ±1.5 V for over 10^5 consecutive ON/OFF cycles for the BRS and CRS devices, showing the high degree of switching repeatability. The insets on the right show expanded views of the SET regions and schematics of the device stacking are shown in the left insets. (c) Electroforming and first switching cycle of a $Pt/TiO_x/TiO_2/Pt$ device, with the device schematic shown in the inset. Even though the device exhibits the BRS behavior, the electroforming process requires +3.1 V and the SET operation requires +1.9 V, in contrast to the lower electroforming-free SET voltages found for the other two device structures.

case, the interface-type switching mechanism largely contributes to the low-power electroforming-free switching, while filamentary switching facilitates the current blockage within a smaller voltage range near 0 V. This new design provides a much more effective solution to mitigate the issue of cross-talk through sneak paths among the neighboring cross-points during high-density cross-bar integration and to prevent the selected cell to be misread due to the neighboring half-selected cell(s). Along with the enhanced switching characteristics at much lower SET and RESET voltages, our CRS device also exhibits a high-performance switching behavior. In Figure 3b, the near overlap of the *IV* curves over 10^5 switching cycles shows the excellent repeatability within the −1.2 to +1.2 V sweep range (with the expanded region near the first SET process shown in the right inset). The magnitude of the two SET voltages for CRS is 650 mV (i.e., $V_{SET(1)}$ = +650 mV and $V_{SET(2)}$ = −650 mV), which is significantly lower than the SET voltage for BRS (+1.1 V). In the case of BRS, the thickness of the TiO_x layer is 50 nm, which requires a higher SET voltage to generate a sufficient electric field for oxygen vacancy diffusion across the oxide matrix. In the CRS device structure, the first 25 nm-thick TiO_x layer can generate a sufficient electric field at the TiO_x/TiO_2 interface even at a lower SET voltage to overcome the barrier height. Once a conducting path is created in the TiO_2 layer, the generated electric field might be enough to expel the oxygen vacancies toward the top electrode, which subsequently leads to a lower observed SET voltage in contrast to that found in a BRS device. It should be noted that even though the ON/OFF current ratio in our CRS structure is slightly smaller than the commercial standard (≥10), this does not affect the endurance and retention behavior of the devices for up to 10^5 cycles with similar LRS and HRS currents. On the other hand, the smaller SET/RESET voltage will help in reducing the power consumption. In a separate experiment, we deliberately fully oxidize the first 25 nm of the TiO_x layer (to TiO_2) to prepare a device with the $Pt/TiO_x/TiO_2/Pt$ architecture (Figure 3c inset). Although the device exhibits a bipolar *IV* characteristic (Figure 3c) due to a thicker TiO_2 layer, this device must undergo a moderate-bias (more than +3.0 V for the 1st cycle) electroforming process for the initial activation before it can be used to perform SET and RESET operations. This is similar to that found for the $Pt/TiO_2/Pt$ structure, which generally requires high-bias electroforming. Pulse measurements are more interesting from the application point of view than analog signals because they are closer to the real input signals in integrated circuits. Our BRS devices have also exhibited a reliable and quick ON/OFF switching performance when digital pulsed voltage signals, analogous to synaptic pulses, are applied. In this short-term potentiation study (Figure S3b), +1.0 V electrical pulses are applied to the device after SET (ON state) and after RESET (OFF state) at an interval of 0.5 ms. The device is also capable of maintaining its current values in the LRS and HRS for an extended testing period of over 10^6 s, with repeated cycling of applying the respective read voltage of +0.8 V to observe the LRS and a successive smaller read voltage of +0.05 V to observe the HRS for a longer interval duration of 600 s (Figure S3c), which demonstrates the outstanding long-term potentiation of the device. We fabricate over 200 cross-bar memristor devices, with a junction size of 10 × 10 μm^2, on the same chip. Figure S4 shows that all these devices exhibit essentially the same switching voltage V_{SET}, which demonstrates the high reproducibility and robustness of our fabrication process.

Recent studies have explored the idea of modulating the switching behavior of memristors under a variety of external parameters, such as stopping voltage, magnetic field, temperature, and illumination conditions.[4,36−39] Figure 4a shows the effect of the stopping voltage V_{STOP} (defined as the maximum positive voltage before reversing the sweep) on the SET voltage of the BRS device. Evidently, both the SET voltage and the ON/OFF current ratio are found to be smaller with a lower V_{STOP}. We also observe an interesting phenomenon when we illuminate the CRS device during electrical measurement with the light of different wavelengths (dark, 254, 302, and 365 nm). Remarkably, the SET voltage can apparently be tuned by the incident light wavelength, with the SET voltage found to decrease with decreasing wavelength of the incident light (Figure 4b). With a higher photon energy, the 254 nm light has produced the smallest SET voltage among other wavelengths, which could be due to the number of photogenerated charges that add to the electrical signal efficiently without disruption caused by signal interference.[38,39]

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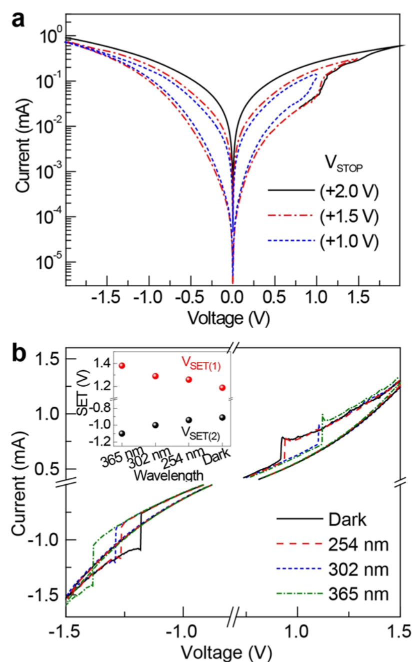

Figure 4. Effect of stopping voltage and UV exposure. (a) *IV* switching behavior of the Pt/TiO_x/Pt device with different $+V_{STOP}$ (maximum positive sweep voltage), with $-V_{STOP}$ kept constant at −2.5 V. By controlling the stopping voltage, it is possible to control the SET and RESET voltages. (b) Different SET voltages for the CRS device under the exposure of UV light of different wavelengths, including dark, 254, 302, and 365 nm, with both V_{SET} values for each wavelength shown in the inset.

A simplified schematic diagram of the proposed CRS mechanism for the Pt/TiO_x/TiO_2/TiO_x/Pt memristor is shown in Figure 5a−h. As there is minimal to no oxygen vacancy in the thin TiO_2 layer, this layer is more resistive in nature, especially when compared to the highly oxygen-deficient TiO_x layers. Prior to any applied bias V (=0), the oxygen vacancies in the TiO_x layers are uniformly distributed across the film, which keeps the device in an HRS (Figure 5a). When a small positive bias is applied to the BE (in the forward sweep), the positively charged oxygen vacancies are pushed toward the TiO_2 layer where they experience a high-resistance barrier (Figure 5b). Once these oxygen vacancies reach to the thin but highly resistive TiO_2 barrier, they tunnel through the barrier at the operating voltage $V_{SET(1)}$ by creating a conducting filamentary path in the TiO_2 layer. At this point, the device switches from the HRS to the LRS for the first time and it stays in the LRS upon further increasing the positive voltage (Figure 5c). When the bias voltage reaches the first RESET voltage $V_{RESET(1)}$, the filamentary path is broken as the oxygen vacancies are completely driven through the TiO_2 layer, reaching the top Pt/TiO_x interface and leaving the TiO_2 layer without any oxygen vacancies, the point at which the device switches back to the HRS (Figure 5d). During the reverse sweep (with the negative bias on the BE and TE at ground), the device stays in the HRS (Figure 5e) until $V_{SET(2)}$, at which a conducting filamentary path is again formed (Figure 5f). Upon the negative bias voltage becoming more negative to $V_{RESET(2)}$ (Figure 5g,h), the device switches back to the HRS. The TiO_x layers are in the HRS during the SET process and then remain in the LRS afterward after the formation of the conducting channel, while the middle TiO_2 layer (being a more resistive oxide) always stays in the HRS. In contrast to the BRS process where the device stays in the LRS upon SET unless RESET is performed by using bias with opposite polarity, the CRS device always stays in the HRS in the lower bias region ($V_{SET(1)} > V > V_{SET(2)}$). It is worth noting that even though the device stays in the HRS in the lower voltage range, the SET voltages are still less than those observed for the BRS device during switching operations. This is due to abundance of oxygen vacancies available after the creation of a filamentary path in the high-resistance barrier layer, which requires less energy to create the interface-conducting path in the top TiO_x layer.

Figure 5i represents the half-read scheme for a cross-bar array due to the sneak path problem in the undesired half-selected cell(s) during data reading from the selected cell. Because all the memory cells of a wordline or bitline are connected in parallel, the access of the selected cell is provided by directly applying the programming voltage (V_P) at BE while keeping TE at ground. This access could also be made through the current path provided by the neighboring cells in a half-voltage scheme. In this case, the neighboring cells will experience an effective voltage of 1/2 V_P that will lead to incorrect output reading from the selected cell, especially when the selected cell is read in the HRS while the neighboring cells are in the LRS. The power consumption will also be the sum of the powers for the selected cell and half-selected cells. To obtain the accurate output reading, there are two approaches: either applying a separate set of biases on the half-selected cells to prevent their unintentional switching from the HRS or creating a complex one-diode one-memory configuration (Figure 5j).[40−42] However, creating a CRS device architecture (Figure 5k) might resolve the issue in a straightforward way because the device always stays in the HRS in a lower voltage range and thus prevents the neighboring cells from induced resistive switching. Our CRS device based on the novel TiO_x/TiO_2/TiO_x double junctions could potentially provide an effective one-step solution to suppress the sneak path problem in the highly interconnected memristor architectures, and it offers more flexibilities in three-dimensional stacking of these memories to overcome the lithography limits.[7] We further calculate the normalized read voltage margin ($\Delta V_{READ}/V_{pu}$) for both of our CRS devices in the worst case scenario using the method described elsewhere.[26,31] In this calculation, the ratio of change in the read voltage (V_{READ}) with respect to the pull-out voltage (V_{pu}) is assumed to be decreased to 10% (Figure S5). The maximum N value is found to be 37 for BRS while that for the CRS device is 66 at the 10% read voltage margin of $\Delta V_{READ}/V_{pu}$. This demonstrates that the TiO_x/TiO_2/TiO_x cross-bar CRS device could be useful for resolving the sneak path problem in ReRAM devices.

■ CONCLUSIONS

We have successfully fabricated two different titanium oxide-based memristors, with remarkably different switching behaviors. The resistive switching characteristic of the Pt/TiO_x/Pt device is bipolar in nature, while that of the Pt/TiO_x/TiO_2/TiO_x/Pt device exhibits unipolar or CRS property. This simple approach of creating CRS memories provides a cost-effective, alternative solution to alleviate the possible sneak-path drawback in high-density cross-bar devices for future electronics, without resorting to more cumbersome solutions of introducing additional components. We also offer a plausible mechanism for CRS in our novel device by considering oxygen

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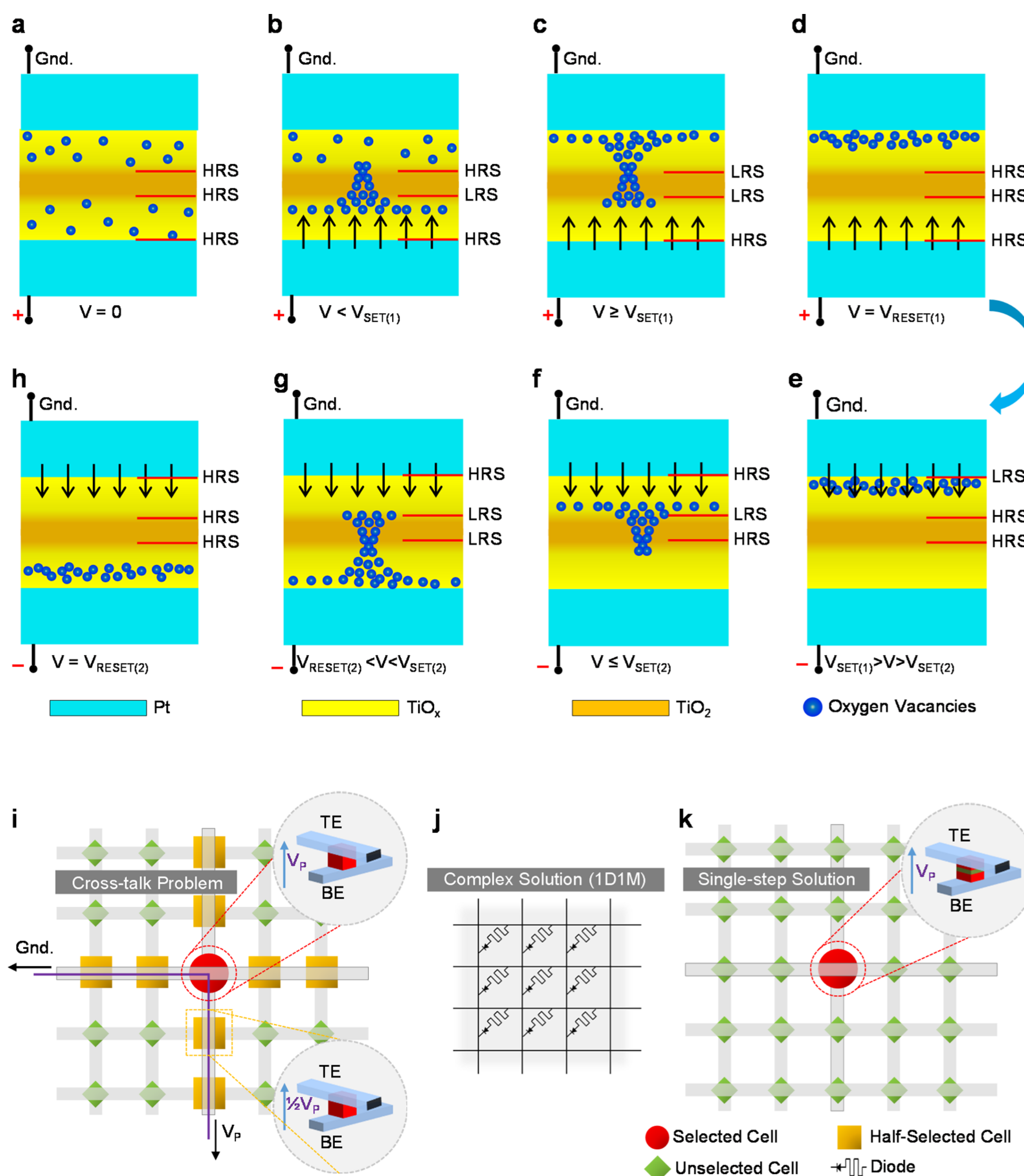

Figure 5. Simplified schematic of the proposed CRS mechanism in a Pt/TiO_x/TiO_2/TiO_x/Pt multilayer device. (a) HRS state of the device prior to any applied bias (oxygen vacancies are uniformly distributed in both TiO_x layers). (b) For $V < V_{SET(1)}$, the oxygen vacancies are driven toward the middle TiO_2 layer. (c) At and above $V_{SET(1)}$, the electric field is sufficiently strong to transport the oxygen vacancies across the TiO_2 layer to the top electrode through the formation of conducting filamentary path(s). (d) At $V_{RESET(1)}$, most of the oxygen vacancies are driven out of the TiO_2 layer onto the top Pt layer. (e−h) A reversible process during the reverse sweep, where similar steps (to a, b, c, and d) are followed through. The schematics are not drawn to scale nor to the thickness ratios. (i) Simple half-read scheme for the cross-bar array application. Each cross-point of a worldline or bitline corresponds to a memory bit. (j) Combination of a cross-bar device structure with additional electronic components such as diodes in a one-diode one-memory configuration to avoid the current leak. (k) Resolution of the cross-talk problem by using the more elegant TiO_x/TiO_2/TiO_x device structure where each cross-point of a worldline or bitline exhibits a complementary resistive memory.

vacancy transport across the multilayer-stacked oxide layers under appropriate bias. The thin TiO_2 layer is the key to restricting the electromigration of oxygen vacancies between the two TiO_x layers at lower voltages. This double-junction CRS device structure provides an elegant one-step solution to the cross-talk problem, potentially paving the way to high volume integration of these cross-bar devices on the same chip. Additionally, we have shown remarkable device stabilities in terms of cyclic repeatability (10^5 cycles) and retention (over 10^6 s). We believe that, given such control over the programming voltage and switching characteristics, this scheme can be of great interest to researchers in the ReRAM community to further explore future application of these device structures.

EXPERIMENTAL SECTION

All the thin film-based cross-bar memristor devices were fabricated on SiO_2/Si substrates using a three-layer maskless photolithography process. 40 nm thick Pt and 50 nm thick oxide films were deposited using magnetron sputtering from Pt and Ti metal targets (99.95% purity, ACI Alloys), respectively, in a PVD chamber. The fabrication and deposition processes are described in detail elsewhere.[15] For the CRS device with TiO_x/TiO_2/TiO_x stacking, a TiO_2 layer was created

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in the middle of the TiO_x stack by exposing the first 25 nm-thick TiO_x layer to the ambient conditions for 24 h to create a few nm-thick TiO_2 layer, before depositing the next 25 nm-thick TiO_x layer. The overall oxide thickness of the three-layer stack remained to be 50 nm.

Surface morphology analysis and elemental mapping were performed by SEM in a Zeiss Merlin microscope coupled with an EDS system. High-resolution cross-sectional TEM analysis was performed in a Zeiss Libra 200MC microscope to illustrate the multilayer stacking and the crystalline nature of the multilayer films. The chemical-state composition of the fabricated device was determined by using XPS in a Thermo-VG Scientific ECSALAB 250 microprobe equipped with a monochromatic Al Kα X-ray source (1486.6 eV). The XPS spectra were fitted with appropriate Voigt functions by using CasaXPS software after removing the Shirley background. The crystalline structures of the as-deposited and annealed TiO_x films were determined by using a PANalytical MRD X'pert Pro X-ray diffractometer with a Cu Kα X-ray source. All the electrical characterization studies on resistive switching, endurance, and retention were performed in *IV* sweep and current−voltage−time (or *IVt*) modes on a Signatone Series 1160 four-probe DC measurement system coupled to an Agilent B1500 semiconductor parameter analyzer.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.1c09775.

> Additional SEM image of memristor cross-bar arrays; XRD profiles of $Pt/TiO_x/TiO_2/TiO_x/Pt$; XPS spectra of the Pt 4f and C 1s regions; retention characteristics and device response to pulse voltage applied for short term and long term; reproducibility of the devices; read margin calculation of the BRS and CRS device structures; and performance comparison of various devices reported in the literature (PDF)

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Notes

The authors declare no competing financial interest.

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